ECTC 2025

75 Years of Pushing the Scale of Connectivity

The 2025 IEEE 75th Electronic Components and Technology Conference

May 27 – 30, 2025

2025 Advance Program

Gaylord Texan Resort & Convention Center
Dallas, Texas, USA

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

Program Supported by

UTECHZONE

For more information visit www.ECTC.net

INTRODUCTION FROM THE IEEE 75TH ECTC PROGRAM CHAIR PRZEMYSLAW GROMALA

The 2025 IEEE 75th Electronic Components and Technology Conference (ECTC) at the Gaylord Texan Resort & Convention Center, Dallas, Texas • May 27 - 30, 2025

On behalf of the Program and Executive Committees, I am delighted to invite you to the IEEE 75th Electronic Components and Technology Conference (ECTC). This premier event, sponsored by the IEEE Electronics Packaging Society, will take place May 27–30, 2025, at the Gaylord Texan Resort & Convention Center in Dallas, Texas. ECTC brings together over 2,000 professionals from across the global microelectronics packaging industry, including manufacturers, design houses, foundries, material suppliers, universities, and investors. Join us to connect with key stakeholders and explore cutting-edge advancements in the field.

The 75th ECTC conference will introduce several new and exciting program events. First, the number of special sessions on Tuesday has more than doubled – from four to nine – with two sessions running in parallel and some really exciting topics and panelists. To support workforce development, we are launching a new student engagement program. We have partnered with local universities and colleges to invite approximately 20 undergraduate students on Wednesday, introducing them to the fascinating world of microelectronics packaging and technologies. Additionally, this year features a student competition challenge. Three winning teams will be invited to the conference to present their projects during Pitch Night, co-organized with the Start-Up Competition Challenge. Lastly, our Thursday ECTC Reception Gala will be expanded with a special event to celebrate the conference's 75th anniversary.

At the 75th ECTC, approximately 400 technical papers will be presented in 36 oral sessions and five interactive sessions. Authors from over 20 countries will share their latest research on topics including 3D integration, bridge and chiplet integration, hybrid bonding, wafer-to-wafer and chip-to-wafer bonding, novel substrate materials, high-density RDL, next-generation interconnections, and warpage management of large panels. Also, large-package manufacturing, additive manufacturing, wearable and medical applications, AI/ML, and advanced RF and antenna design are on the agenda. Thermal management, interconnect reliability, advanced characterization, and process simulations, eco-friendly packaging, and secure designs will be discussed as well. Interactive sessions will focus on innovations in bonding, power delivery, optimization algorithms, specialized device packaging, and reliability testing. The 75th ECTC serves as a global platform for exploring cutting-edge advancements in microelectronic packaging, fostering innovation, and addressing industry challenges.

This year, the conference features a total of eleven special sessions with industry experts, including nine on Tuesday, each lasting 90 minutes. On Tuesday, two parallel sets of special sessions take place instead of one as in previous years. Rozalia Beica (Rapidus) and Habib Hichri (Ajinomoto Fine-Techno USA) chair the first session, which explores Ultra High-Density Interconnect Technologies. Mascha Gorchichko (Applied Materials) and Dishit Parekh (AMD) chair the second session, focusing on Hybrid Bonding. At 10:30 a.m., Richard Pitwon (Resolute Photonics Ltd) and Ajey Jacob (University of Southern California) discuss Quantum Advanced Packaging. Simultaneously, Jan Vardaman (TechSearch International), Zia Karim (Yield Engineering Systems), and Thom Gregorich (Zeiss) will present on Glass Core vs. RDL Interposers. In the afternoon, Vidya Jayaram (Chipletz) and Karan Bhangaonkar (Google) will chair a session on Advanced Materials for Co-Packaged Optics. For those interested in Fault and Failure Analysis in Chiplets, Yan Li (Samsung), Tae-Kyu Lee (Cisco), and Zhi Yang (Groq) simultaneously lead a dedicated session. The final two special session blocks include a discussion on Sub-THz Packaging for Communication and Radar, chaired by Maciej Wojnowski (Infineon Technologies AG) and Ivan Ndip (Fraunhofer IZM/Brandenburg University of Technology), as well as a session on Thermal Management for Power Delivery, chaired by Dwayne Shirley (Marvell) and Tiwei Wei (Purdue University).

Parallel to the special sessions, the Heterogeneous Integration Roadmap (HIR) workshop will be chaired by William Chen (ASE) and Ravi Mahajan (Intel). Four sessions are planned: IoT & AI at the Edge, moderated by Wei Chung Lo (ITRI) and Rockwell Hsu (Cisco); Advancing Heterogeneous Integration through Metrology & Ai, moderated by Chris Bailey (ASU) and Xuejun Fan (Lamar University); Integrating Photonics in HPC & Network Systems, moderated by Kanad Ghose (Binghamton Univ.) and John Shalf (LBL); and Advances in Panels, Substrates and Printed Circuit Boards moderated by William Chen (ASE) and Ravi Mahajan (Intel).

Tuesday evening offers additional opportunities to engage. Aakrati Jain (IBM) will lead a Young Professionals Networking Event from 6:45 p.m. to 7:45 p.m., featuring a new fish-bowl discussion format. Following this, Takashi Hisada and Yasumitsu Orii (both with Rapidus) will chair the IEEE EPS Seminar on User Perspectives of Chiplet Technology from 7:45 p.m. to 9:15 p.m.

On Wednesday morning, May 28, 2025, ECTC will feature a keynote presentation on Achieving Efficient Zettascale Compute in the AI Era by Sam Naffziger (AMD), invited by General Chair Florian Herrault (PseudolithIC, Inc.) The Student Engagement Program, chaired by Ibrahim Guven (Virginia Commonwealth University), will also take place throughout the day, welcoming undergraduate students from local universities and colleges. On Thursday, May 29, 2025, from 8:00 to 9:15 a.m., a Plenary Session on Emerging Advanced Power Delivery for the AI Computing Era will be chaired by Dongming He (Qualcomm) and Eric Beyne (imec). Additionally, an IEEE EPS President's panel titled ECTC at 75: Celebrating the Past, Innovating for the Future organized by IEEE EPS President Patrick Thompson (Texas Instruments) will be held on Friday morning, May 30, 2025.

The IEEE ITherm Conference is co-located with the 75th Anniversary ECTC and co-organizes 16 CEU-approved Professional Development Courses (PDCs). Organized by Kitty Pearsall and Jeffrey Suhling, these expert-led courses will be held on Tuesday, May 27, 2025.

The ECTC Exhibits, running Wednesday, May 28, and Thursday, May 29, showcase cutting-edge technologies and products from over 100 leading companies in electronic components, materials, packaging, and services. Starting daily at 9 a.m., the exhibits provide excellent opportunities for networking during coffee breaks, luncheons, and evening receptions.

Whether you are an engineer, manager, student, or executive, ECTC offers unique experiences for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the Anniversary 75th ECTC and to be a part of all the exciting technical and professional opportunities.

I want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the Anniversary 75th ECTC a success. I look forward to meeting you at the Gaylord Texan Resort & Convention Center, Dallas, Texas, from May 27 to 30, 2025.

Przemyslaw Gromala
75th ECTC Program Chair
pgromala@ieee.org

Index

75th ECTC ADVANCE REGISTRATION

Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions see page 32.

Register by May 1, 2025 and save US$100 or more! All registrations received thereafter are considered Door Registrations. Those who register in advance can print out their badges and pick up their registration packets at the ECTC Registration Desk in the Convention Center Lobby.

On-Site Registration Schedule

Registration will be held in the Convention Center Lobby

Monday, May 26, 2025	12:00 Noon – 4:00 p.m.
Tuesday, May 27, 2025	6:45 a.m. – 7:45 p.m.*

**6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Sessions only*

Wednesday, May 28, 2025	6:45 a.m. – 4:00 p.m.
Thursday, May 29, 2025	7:00 a.m. – 4:00 p.m.
Friday, May 30, 2025	7:00 a.m. – 12:00 Noon

The schedule for Tuesday will be rigorously enforced to prevent PDC attendees from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The Gaylord Texan Resort & Convention Center, as well as ECTC, are both smoke-free environments.

ITherm 2025

ITherm is co-located with ECTC! All ITherm sessions and exhibits will take place in the Gaylord Texan Resort & Convention Center. For more information about ITherm 2025 please visit **https://www.ieee-itherm.net/**.

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

ECTC Sponsors

With over seven decades of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 2,000 individuals and more than 150 organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company's interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors".

To sign-up for sponsorship or to get more details, please contact Alan Huffman at **alan.huffman@ieee.org or +1-336-380-5124.**

Hotel Accommodations

Rooms for ECTC attendees have been reserved at the Gaylord Texan Resort & Convention Center. The special conference rate for a single/double occupancy room is:

US $229.00 per night
This price includes single or double occupancy in one room.

Please note these rooms are on a first come, first serve basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Room reservations must be made directly with the hotel by May 1, 2025, at 5 p.m., Central Daylight Time (CDT), or until rooms run out, whichever comes first, to ensure our special conference rate. All reservations made after the cutoff date or after rooms run out will be accepted on a space and rate availability basis. If you need to cancel a reservation, please do so by 5 p.m. Central Time at least 5 days prior to arrival for a full refund.

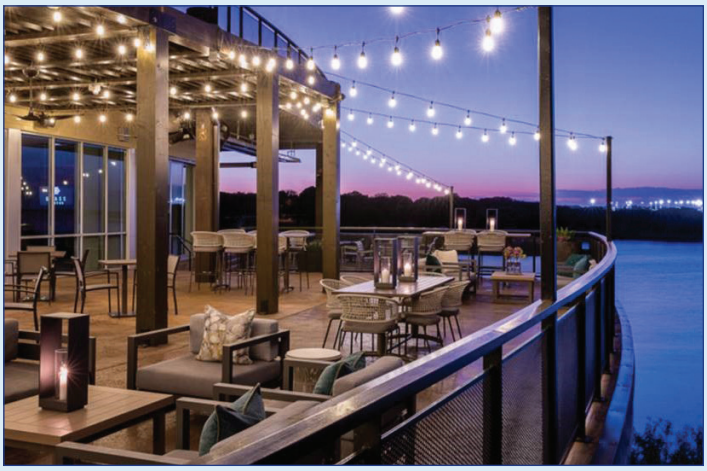
Check-in time is 4 p.m. and check-out time is 11 a.m.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2025 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2025 from 3rd party companies. These emails and sites are likely scams and not to be trusted. **The only formal communication** ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee or our IT system. **ECTC's only authorized site** for reserving a room is through our website **(www.ectc.net)**. Should you have any questions about booking a hotel room please contact ECTC staff at: **registration@ectc.net**

Transportation Services

There is no complimentary transportation to and from the hotel and airport. All attendees must make their own transportation arrangements to the hotel upon arriving at the airport.



75th ECTC CONFERENCE OVERVIEW

2025 Special Session on Ultra High Density Interconnect Technologies

Ultra High Density Interconnect Technologies and Supply Chain Readiness for AI & HPC

Tuesday, May 27, 2025, 8:30 a.m. – 10:00 a.m.

Chairs: Rozalia Beica, Rapidus and Habib Hichri, Ajinomoto Fine-Techno USA Corporation


Heterogeneous integration and chiplets will require fine line and space interconnects, as well as low warpage materials, to achieve the required performance for various applications in the rapidly evolving landscape of Artificial Intelligence (AI) and High-Performance Computing (HPC), which have significantly increased computational and memory needs. One of the critical areas that continues to have challenges in the industry is advancing the interconnects at the organic substrate level, reason why various different approaches are being considered:

- Ultra-high density organic substrate (2.0D), bringing front-end of the line processes into the substrate/panel infrastructure to meet ultrafine Via/L/S (2/2/2 um and below).
- Building the organic substrate at wafer level (SOW)
- Hybrid substrates
- Bringing the well-known redistribution lines (RDLs) to substrates using 2.xD technologies
- Bringing glass substrates to address the needs for advanced interconnects and warpage issues for large size and complex substrates.

Each of these approaches have their own limitations and challenges. This session will discuss the different alternative technologies addressing the latest developments and remaining challenges, supply chain readiness to address the next generation of interconnects.

The session will comprise a panel of industry experts across the supply chain with global participation. Each panelist will provide a short presentation of their view on these technologies and supply chain readiness followed by a panel discussion.

Yu Hua Chen, Unimicron; Niranjan Khasgiwale, Applied Materials; Kuldip Johal, Atotech; Yoshio Nishimura, Ajinomoto; Monita Pau, Onto Innovation; Yoshio Takatsu, ORC Manufacturing Co., Ltd.

2025 Special Session on Hybrid Bonding

Hybrid Bonding (HB): to B, or not to B? Needs and challenges for the Next Decade

Tuesday, May 27, 2025, 8:30 a.m. – 10:00 a.m.

Chairs: Mascha Gorchichko, Applied Materials, Inc. and Dishit Parekh, AMD


Hybrid bonding is the key technology for high-density 3D integration and advanced packaging. In recent years, significant advancements were made in pitch scaling, die-to-die bonding, alternative materials, and low-temperature processes. However, there are still engineering and technological challenges that need to be addressed to expand the application domain, such as defectivity, metrology, design challenges, and costs.

This panel aims to summarize the recent advancements in hybrid bonding, identify the most pressing issues limiting the adoption of this technology for mainstream electronics, and outline the expected development of this technology for the next decade.

Sujin Ahn, Samsung Electronics; Liwei Wang, AMD; Chet Lenox, KLA Corporation; Anne Jourdain, imec; Masao Tomikawa, Toray Industries, Inc.; Laura Mirkarimi, Adeia

2025 Special Session on Quantum Packaging

Quantum Photonic Advanced Packaging

Tuesday, May 27, 2025, 10:30 a.m. – 12:00 p.m.

Chairs: Richard Pitwon, Resolute Photonics Ltd. and Ajey Jacob, University of Southern California


As quantum technologies advance, the need for robust and scalable systems to support applications like Quantum Key Distribution (QKD) and quantum photonic computation becomes increasingly critical. These emerging technologies demand a sophisticated ecosystem capable of integrating high-fidelity quantum photonic systems into the quantum physical layer, where single or entangled photon qubits are conveyed and processed. Quantum photonic systems, by their nature, require exceptional precision and control at the quantum level, which necessitates the heterogeneous integration of diverse materials and technologies into a cohesive unit that functions seamlessly. This integration is vital for ensuring the accurate transmission and manipulation of quantum information, which is the cornerstone of quantum computing and secure quantum communication. In this session, we will explore the latest advances in the assembly and packaging of quantum photonic systems. The focus will be on how innovative packaging solutions can address the unique challenges posed by quantum technologies, such as minimizing photon loss, ensuring thermal stability, transduction schemes, and maintaining the coherence of quantum states. We will discuss how these packaging techniques are being developed to support the high volume manufacturing of quantum devices, enabling their widespread adoption of data centric industries.

Bernard Lee, Senko; Michael Fanto, Air Force Research Lab; Takahiro Kashiwazaki, NTT; Inna Krasnokutska, Xanadu Quantum Technologies Inc.

2025 Special Session on Glass Core vs. RDL Interposers

Glass Core vs. RDL Interposers: Ready for Prime-Time?

Tuesday, May 27, 2025, 10:30 a.m. – 12:00 p.m.

Chairs: Jan Vardaman, TechSearch International, Inc., Zia Karim, Yield Engineering Systems, and Thom Gregorich, Zeiss



Given the critical role of high-density substrates in the semiconductor industry, glass-core substrates and RDL interposer advantages have been discussed. With growing demand for higher performance, larger devices, and increased interconnect density, where does each technology fit, what are the necessary steps to address the critical challenges faced by the entire industry?

This session will address economic and technical perspectives for high volume solutions, including design, materials, process/equipment, and metrology to meet product needs and reliability requirements. The session will include a moderator and six panelists.

Brett Wilkerson, AMD; Kathy Yan, TSMC; Duan Gang, Intel Corp.; Richard Bae, Samsung; Akira Tamura, FICT; Makoto Kouzuma, Toppan

2025 Special Session on Advanced Materials for Co-Packaged Optics

Advanced Materials for Enabling Co-Packaged Optics Integration

Tuesday, May 27, 2025, 1:30 p.m. – 3:00 p.m.

Chairs: Vidya Jayaram, Chipletz and Karan Bhangaonkar, Google


Modern computing techniques are pushing the boundaries for high performance requirements. Co-packaged optics emerged as the future of microelectronics packaging, integrating optics and electronics on a single substrate, to meet the computing and communication demands for high bandwidth at low power. Although there are numerous challenges in realizing the optical co-packaging technology, what comes along are great opportunities for foundries, IDMs and OSATs. Materials and processes play a key role in enabling this disruptive technology. Thus, this special session will invite industry leaders to share their insight about the innovations, challenges and future needs in realizing CPO technology.

Christopher Striemer, AIM Photonics; Padraic Morrissey, Tyndall Institute; Mark Gerber, ASE; Kumar Abhishek Singh, Intel; Rena Huang, Rensselaer Polytechnic Institute

2025 Special Session on Fault and Failure Analysis in Chiplets

Advances in Chiplets: Tackling Fault Isolation and Failure Analysis in Heterogeneous Integration

Tuesday, May 27, 2025, 1:30 p.m. – 3:00 p.m.

Chairs: Yan Li, Samsung, Tae-Kyu Lee, Cisco Systems, Inc., and Zhi Yang, Groq



By providing timely feedback data for effective failure root cause investigation, problem solving proposal and validation, process technology improvement, yield enhancement, and reliability risk assessment, Fault Isolation (FI) and Failure Analysis (FA) play a crucial role during the technology development of Heterogeneous Integration, which is the leading advanced packaging technology developed to meet the High-Performance Computing (HPC) and Artificial Intelligence (AI) market demands of ever higher performance, lower power consumption, wider memory bandwidth with reduced latency. During the panel discussion, experts from both industry and academia will discuss the technology gaps and novel methodologies and techniques in FI and FA of Heterogeneous Integration.

Dr. Lihong Cao, ASE; Dr. Wenbing Yun, Sigray; Dr. Bernice Zee, AMD Singapore; Prof. Navid Asadi, University of Florida; Yaw S. Obeng, NIST; Dr. Thomas Rodgers, Zeiss

2025 Special Session on Thermal Management for Power Delivery

Thermal Management Solutions for Next-Generation Backside Power Delivery

Tuesday, May 27, 2025, 3:30 p.m. – 5:00 p.m.

Chairs: Dwayne Shirley, Marvell Semiconductor, Inc. and Tiwei Wei, Purdue University


The increasing power density and thermal challenges in advanced semiconductor packaging have led to the development of backside power delivery (BPD) technology. BPD relocates the power delivery network from the frontside to the backside of a silicon wafer, enhancing power efficiency, performance, and design flexibility. However, this technology also introduces new thermal management challenges, including higher thermal densities and the need for innovative cooling solutions.

This special session aims to bring together experts from academia and industry to discuss the latest advancements and challenges in thermal management solutions for next-generation BPD.

Dureseti Chidambarrao, IBM; Muhannad S Bakir, GA Tech; Herman Oprins, imec; Rongmei Chen, Peking University

2025 Special Session on Sub-THz Packaging for Communication and Radar

Advancements in mmWave and Sub-THz Packaging for Communication and Radar Applications

Tuesday, May 27, 2025, 3:30 p.m. – 5:00 p.m.

Chairs: Maciej Wojnowski, Infineon Technologies AG and Ivan Ndip, Fraunhofer IZM/Brandenburg University of Technology


In this session, experts from industry and academia will present the latest developments in high-frequency packaging and system integration at mmWave and sub-THz frequency bands. The session will begin with presentation of emerging wireless communication and radar sensing applications in these bands, and resulting challenges and opportunities for RF packaging. Advanced system integration platforms using different high-frequency materials for these applications will be presented. Emphasis will be laid on characterizing the packaging materials and interconnects at these very high frequencies as well as on co-design and co-simulation techniques. The session will conclude with presentation and discussion of concrete examples of latest developments of novel interconnects, components and wireless modules for 6G communication and radar applications at mmWave and sub-THz bands.

Madhavan Swaminathan, Penn State University; Xiao Sun, imec; Parisa Aghdam, Ericsson; Atom Watanabe, IBM T.J. Watson Research Center

2025 IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop

Four Technical Sessions, spanning morning and afternoon of Tuesday, May 27, 2025

Chairs: Ravi Mahajan, Intel Corporation and William Chen, ASE


HIR Welcome, Introduction & Agenda Review

IoT & AI at the Edge

Advancing Heterogeneous Integration through Metrology & AI

Integrating Photonics in HPC & Network Systems

Advances in Panels, Substrates and Printed Circuit Boards

2025 ECTC Young Professional Networking Event

Tuesday, May 27, 2025, 6:45 p.m. – 7:45 p.m.

Chair: Aakrati Jain, IBM

Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2025 IEEE EPS Seminar on Chiplet Technology

User Perspective of Chiplet Technology

Tuesday, May 27, 2025, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada, Rapidus and Yasumitsu Orii, Rapidus


Styled as a start-up competition, this session looks at next generation materials and companies.

The EPS Seminar organized by the technical committee TC6 (High-Density Substrate and Board) of IEEE EPS will discuss the current status and future evolution of chiplet technology from the end use perspective. We will have 5 panelists from various segments such as high-end computing, automotive and network. Each panelist will give a short talk presenting insights on technical trends/challenges including optically integrated chiplet, application requirements, user's expectation of chiplet technology, followed by a panel discussion.

Raja Swaminathan, AMD; Takao Iwaki, ASRA (MIRISE Technologies); Takashi Saida, NTT: Omar Bchir, Qualcomm; Carlos Macian Ruiz, Marvell; Sam Karikalan, Broadcom.

2025 ECTC Keynote Talk

Achieving Efficient Zettascale Compute in the AI Era

Wednesday, May 28, 2025, Time: 8:00 a.m. – 9.15 a.m.

Chair: Florian Herrault, PseudolithIC Inc.
Speaker: Sam Naffziger, AMD


The demand for compute and the energy to power it is increasing faster than ever before in our industry. Meeting the challenge of delivering this processing power in the AI era requires holistic innovation from the device to the datacenter level. It starts with integrating highly optimized, domain-specific accelerators with advanced 2.5D and 3.5D packaging to maximize the amount of compute within the most efficient, local communication domain. These accelerators and other system components must be packed into tightly integrated sleds that minimize losses and power for high-speed communication while taking advantage of workload-aware power management. Scaling to the rack and datacenter level will require many advances in signaling technologies, rack design, and power optimization to enable the training and inference computation required by the most demanding frontier models. This talk will cover these trends and key technologies that will power compute growth at a scale we wouldn't have conceived of just a few short years ago.

These sessions are open to all conference attendees.

2025 ECTC Student & Start-Up Innovation Challenge

Future Forward: The Student & Start-up Innovation Challenge!

Wednesday, May 28, 2025, 6:30 p.m. - 8:30 p.m.

Chairs: Rozalia Beica, Rapidus, Farhang Yazdani, BroadPak, and Jason Rouse, Taiyo America, Inc.



This session is organized as a competition and will have competing pitches of both student teams and start-ups followed by deliberation of a jury panel, awards announcements, and networking session. We will have three student pitches and six start-up pitches (7 min. each) followed by Q&A from the jury panel. The Q&A will be open to the audience. The jury will deliberate and choose the winning student team and start-up. The session will end with the announcement of the winners and a networking session.

2025 Plenary Session on Advanced Power Delivery for AI

Emerging Advanced Power Delivery for the AI Computing Era

Thursday, May 29, 2025, 8:00 a.m. – 9:15 a.m.

Chairs: Dongming He, Qualcomm Technologies, Inc. and Eric Beyne, imec


AI computing introduces significant challenges for energy consumption and thermal management. Optimal power delivery network (PDN) is crucial for CPU, GPU and NPU power and performance. Advanced PDN solutions such as silicon deep trench capacitor (DTC) and integrated stacked capacitor (ISC), integrated voltage regulator (IVR), silicon metal-insulator-metal (MIM) capacitor and thin film inductor, backside power rail, etc., have been explored, developed, and adopted. Industry leaders and experts will share their views on benefit and tradeoff for these building blocks, integration challenges and opportunities at silicon device, package and board levels plus system technology co-optimization (STCO).

Kaladhar Radhakrishnan, Intel Corp.; Harrison Chang, ASE Global; PR. Chidi Chidambaram, Qualcomm; Raja Swaminathan, AMD; Chuei-Tang Wang, TSMC

2025 IEEE EPS President's Panel

ECTC at 75: Celebrating the Past, Innovating for the Future

Friday, May 30, 2025, 8:00 a.m. – 9:15 a.m.

Chair: Patrick Thompson, Texas Instruments

Join EPS/ECTC luminaries as they share:

- Early memories of ECTC and key innovations that revolutionized the industry
- What's happening now that is exciting to them
- Their thoughts on what we'll be reviewing at the 100th ECTC

Luncheons

ECTC offers a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. The QR code on your registration badge will scan you into lunch. Please come and enjoy time with other attendees and colleagues in the industry! Lunch times vary, see below for specific details for each day.

Tuesday:	**12:00 Noon – 1:15 p.m.**
Wednesday:	**12:45 p.m. – 2:00 p.m.**
Thursday:	**12:45 p.m. – 2:00 p.m. – Sponsored by: The IEEE Electronics Packaging Society (EPS)**
Friday:	**12:45 p.m. – 2:00 p.m. – Don't miss out on this lunch! We will be raffling off a number of prizes including a hotel stay, free conference registrations, and many other industry gadgets!**

ECTC Student Reception

Tuesday, May 27, 2025 • 5:00 p.m. – 6:00 p.m.

Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise!

General Chair's Speakers Reception

Tuesday, May 27, 2025 • 6:00 p.m. – 7:00 p.m.

(by invitation only)

Exhibitor Reception

Wednesday, May 28, 2025 • 5:30 p.m. – 6:30 p.m.

EPS Chapter Officer Meet and Greet

Thursday, May 29, 2025 • 7:00 a.m. – 8:00 a.m.

(online by invitation)

With 46 EPS Chapters all over the world, this once-a-year event is a great opportunity for all chapter officers to meet with fellow officers face to face and to learn about successes and best practices.

Program Director: Andrew Tay
Regions 1-7 and 9 (Americas): Annette Teng
Region 8 (Europe and Africa): Steffen Kroehnert
Region 10 (Asia): Wong Shaw Fong

75th ECTC Gala Reception

Thursday, May 29, 2025 • 7:30 p.m.

Hosted by Koh Young Technology

Please note: Badges are required for the duration of the conference including all evening functions and receptions.

Executive Committee

Chair
Florian Herrault
PseudolithIC, Inc.
floherrault@gmail.com

Vice-General Chair
Michael Mayer
University of Waterloo
mmayer@uwaterloo.ca

Program Chair
Przemyslaw Gromala
Robert Bosch GmbH
pgromala@ieee.org

Assistant Program Chair
Bora Baloglu
Intel Corporation
borabal@ieee.org

Jr. Past General Chair
Karlheinz Bock
TU Dresden
karlheinz.bock@tu-dresden.de

Sr. Past General Chair
Ibrahim Guven
Virginia Commonwealth University
iguven@vcu.edu

Sponsorship Chair
Alan Huffman
L3Harris
alan.huffman@ieee.org

Finance Chair
Patrick Thompson
Texas Instruments, Inc.
patrick.thompson@ti.com

Publications Chair
Henning Braunisch
Intel Corporation
braunisch@ieee.org

Publicity Chair
Eric Perfecto
IBM Research
eric.perfecto.us@ieee.org

Treasurer
Tom Reynolds
T3 Group LLC
t.reynolds@ieee.org

Exhibits Chair
Sam Karikalan
Broadcom Limited
samkarikalan@ieee.org

IT Coordinator
Tanja Braun
Fraunhofer IZM
tanja.braun@izm.fraunhofer.de

Professional Development Course Chair
Kitty Pearsall
Capstan Technologies
kitty.pearsall@gmail.com

Conference Management
Lisa Renzi Ragar
Renzi & Company, Inc.
lrenzi@renziandco.com

IEEE EPS Representative
Annette Teng
AIM Photonics
ateng@sunypoly.edu

Packaging Technologies

Chair
Mike Gallagher
DuPont Electronic Materials
michael.gallagher@dupont.com

Assistant Chair
Peng Su
Juniper Networks
pensu@juniper.net

Lihong Cao
Advanced Semiconductor Engineering, Inc.
lihong.cao@aseus.com

Jie Fu
Apple Inc.
fujie6@gmail.com

Glenn Ning Ge
TetraMem
glenn.ge@tetramem.com

Kuldip Johal
MKS Instruments - MSD
kuldip.johal@atotech.com

Sam Karikalan
Broadcom Limited
samkarikalan@ieee.org

Beth Keser
Zero ASIC
bethk@kesers.com

Young-Gon Kim
Renesas Electronics America
young.kim.jg@renesas.com

Andrew Kim
Apple
hkim34@apple.com

John Knickerbocker
IBM Corporation
knickerj@us.ibm.com

Steffen Kroehnert
ESPAT Consulting, Germany
steffen.kroehnert@espat-consulting.com

Albert Lan
Applied Materials
Albert_Lan@amat.com

John H. Lau
Unimicron Technology Corporation
John_Lau@Unimicron.com

Jaesik Lee
SK Hynix USA
Jaesik.Lee@us.skhynix.com

Kyu-Oh Lee
Intel Corporation
kyu-oh.lee@intel.com

Markus Leitgeb
AT&S
m.leitgeb@ats.net

Monita Pau
Onto Innovation
monita.pau@ontoinnovation.com

Luu Nguyen
Psi Quantum
lnguyen@psiquantum.com

Raj Pendse
Facebook
rajd@fb.com

Min Woo Rhee
Samsung
mw.daniel.lee@gmail.com

Subhash L. Shinde
Notre Dame University
sshinde@nd.edu

Joseph W. Soucy
Draper Laboratory
jsoucy@draper.com

Eric Tremble
Marvel
etremble@marvell.com

Kuo-Chung Yee
Taiwan Semiconductor Manufacturing Corporation, Inc.
kcyee@tsmc.com

Applied Reliability

Chair
Vikas Gupta
ASE US, Inc
Gvikas.Gupta@outlook.com

Assistant Chair
Sandy Klengel
Fraunhofer Institute for Microstructure of Materials and Systems
sandy.klengel@imws.fraunhofer.de

Seung-Hyun Chae
SK Hynix
seunghyun1.chae@sk.com

Tz-Cheng Chiu
National Cheng Kung University
tcchiu@mail.ncku.edu.tw

Deepak Goyal
Intel Corporation
deepak.goyal@intel.com

Nokibul Islam
JCET Group
Nokibul.islam@jcetglobal.com

Choong-Un Kim
The University of Texas at Arlington
choongun@uta.edu

Tae-Kyu Lee
Cisco Systems, Inc.
taeklee@cisco.com

Yan Li
Samsung Semiconductor Inc.
yan.a.li@samusung.com

Pilin Liu
Intel Corporation
pilin.liu@intel.com

Varughese Mathew
NXP Semiconductors
varughese.mathew@nxp.com

Keith Newman
AMD
keith.newman@amd.com

Donna M. Noctor
Nokia
donna.noctor@nokia.com

S. B. Park
Binghamton University
sbpark@binghamton.edu

Scott Savage
Medtronic Microelectronics Center
scott.savage@medtronic.com

Jeffrey Suhling
Auburn University
jsuhling@auburn.edu

Paul Tiner
Texas Instruments
p-tiner@ti.com

Pei-Haw Tsao
Mediatek
ph.tsao@mediatek.com

Dongji Xie
NVIDIA Corporation
dongjix@nvidia.com

Assembly & Manufacturing Technology

Chair
Paul Houston
Engent
paul.houston@engentaat.com

Assistant Chair
Christo Bojkov
UT Dallas
cbojkov.ectc@gmail.com

Sai Ankireddi
Maxim Integrated
sai.ankireddi@alumni.purdue.edu

Pascale Gagnon
IBM Canada
pgagnon@ca.ibm.com

Mark Gerber
Advanced Semiconductor Engineering, Inc.
mark.gerber@aseus.com

Omkar Gupte
AMD
Omkar.Gupte@amd.com

Timo Henttonen
Microsoft
timo.henttonen@microsoft.com

Habib Hichri
Ajinomoto Fine-Techno USA Corporation
hichrih@ajiusa.com

Li Jiang
Texas Instruments
l-jiang1@ti.com

Zia Karim
Yield Engineering Systems
ZKarim@yes.tech

Wei Koh
Pacrim Technology
kohmail@gmail.com

Siddarth Krishnan
Applied Materials
sidkris@gmail.com

Wenhao (Eric) Li
Intel Corporation
wenhao.li@intel.com

Venkata Mokkapati
AT & S
v.mokkapati@ats.net

Jae-Woong Nah
IBM Corporation
jnah@us.ibm.com

Valerie Oberson
IBM Canada Ltd
voberson@ca.ibm.com

Jason Rouse
Taiyo America, Inc.
jhrouse@taiyo-america.com

Andy Tseng
Qualcomm Technologies, Inc.
andytseng2000@yahoo.com

Jobert Van Eisden
MKS Instruments
Jobert.van-Eisden@atotech.com

Jan Vardaman
TechSearch International
jan@techsearchinc.com

Shaw Fong Wong
Intel Corporation
shaw.fong.wong@intel.com

Jin Yang
Samsung Electronics
jin1.yang@ieee.org

Cong Zhao
Meta
zhaocong@meta.com

Ralph Zoberbier
Evatec AG
ralph.zoberbier@evatecnet.com

Interactive Presentations

Chair
Frank Libsch
IBM Corporation
libsch@us.ibm.com

Assistant Chair
Karan Bhangaonkar
Google
karanbhangaonkar@outlook.com

Rao Bonda
Amkor Technology
rao.bonda@amkor.com

Joshua Dillon
Marvell Govt. Solutions
JoshuaFDillon@gmail.com

Mark Eblen
Kyocera International SC
mark.eblen@kyocera.com

Mohammad Enamul Kabir
Intel Corporation
enamul101b@yahoo.com

Ibrahim Guven
Virginia Commonwealth University
iguven@vcu.edu

Alan Huffman
L3Harris
alan.huffman@ieee.org

Jeffrey Lee
iST-Integrated Service Technology Inc.
jeffrey_lee@istgroup.com

Stephen Lee
NXP Semiconductors
stephen.lee@nxp.com

Michael Mayer
University of Waterloo
mmayer@uwaterloo.ca

Saikat Mondal
Intel Corporation
saikat.mondal@intel.com

Pavel Roy Paladhi
NVIDIA
rpaladhi01@gmail.com

Mark Poliks
Binghamton University
mpoliks@binghamton.edu

Patrick Thompson
Texas Instruments, Inc.
patrick.thompson@ti.com

Kristina Young
Synopsys Inc
kristina.youngfisher@gmail.com

Interconnections

Chair
Ou Li
Advanced Semiconductor Engineering, Inc.
ou.li@aseus.com

Assistant Chair
Gang Duan
Intel
gang.duan@intel.com

Jian Cai
Tsinghua University
jamescai@tsinghua.edu.cn

C. Key Chung
TongFu Microelectronics Co. Ltd.
chungckey@hotmail.com

David Danovitch
University of Sherbrooke
David.Danovitch@USherbrooke.ca

Bernd Ebersberger
Infineon Technologies
bernd.ebersberger@infineon.com

Takafumi Fukushima
Tohoku University
fukushima-tak@tohoku.ac.jp

Thom Gregorich
Carl Zeiss
tmgregorich@gmail.com

Yoshihisa Kagawa
Sony
Yoshihisa.Kagawa@sony.com

Seung Yeop Kook
GlobalFoundries
seung-yeop.kook@globalfoundries.com

Kangwook Lee
SK Hynix
steward.lee@sk.com

Li Li
Infinera
packaging@yahoo.com

Changqing Liu
Loughborough University
c.liu@lboro.ac.uk

Wei-Chung Lo
ITRI, Industrial Technology Research Institute
lo@itri.org.tw

Nathan Lower
Consultant
nplower@hotmail.com

James Lu
Rensselaer Polytechnic Institute
luj@rpi.edu

Vempati Srinivasa Rao
IME A-star
vempati@ime.a-star.edu.sg

Katsuyuki Sakuma
IBM Research
ksakuma@us.ibm.com

Jean-Charles Souriau
CEA Leti
jcsouriau@cea.fr

Chuan Seng Tan
Nanyang Technological University
tancs@alum.mit.edu

Chih-Hang Tung
Taiwan Semiconductor Manufacturing Company
chtungc@tsmc.com

Tiwei Wei
Purdue University
tiwei@purdue.edu

Matthew Yao
GE Aerospace
matthew.yao@ge.com

Chaoqi Zhang
Qualcomm Technologies, Inc.
chaoqi.gt.zhang@gmail.com

Dingyou Zhang
Broadcom Inc.
dingyouzhang.brcm@gmail.com

Wei Zhou
Micron
zhouwei@micron.com

Materials & Processing

Chair
Qianwen Chen
Broadcom
wendy.chen@broadcom.com

Assistant Chair
Vidya Jayaram
Intel Corporation
vidya.jayaram@intel.com

Tanja Braun
Fraunhofer IZM
tanja.braun@izm.fraunhofer.de

Yu-Hua Chen
Unimicron
yh_chen@unimicron.com

Jae Kyu Cho
GlobalFoundries
jaekyu.cho@globalfoundries.com

Bing Dang
IBM Corporation
dangbing@us.ibm.com

Gibran Liezer Esquenazi
LQDX
gibranesquenazi@gmail.com

Lewis Huang
Senju Electronic
lewis@senju.com.tw

C. Robert Kao
National Taiwan University
crkao@ntu.edu.tw

Alvin Lee
Brewer Science
alee@brewerscience.com

Yi Li
Intel Corporation
yi.li@intel.com

Ziyin Lin
Intel Corporation
ziyin.lin@intel.com

Yan Liu
Medtronic Inc. USA
yan.x.liu@medtronic.com

Mikel Miller
Apple Inc.
mikel_miller@apple.com

Praveen Pandojirao-S
Johnson & Johnson
praveen@its.jnj.com

Mark Poliks
Binghamton University
mpoliks@binghamton.edu

Dwayne Shirley
Marvell Semiconductor, Inc.
shirley@ieee.org

Ivan Shubin
Raytheon Technologies
ishubin@gmail.com

Bo Song
HP Inc.
bo.song@hp.com

Yoichi Taira
Keio University
taira@appi.keio.ac.jp

Frank Wei
DISCO Corporation
frank_w@discousa.com

Lingyun (Lucy) Wei
Dupont
lingyun.wei@dupont.com

Kimberly Yess
Brewer Science
kyess@brewerscience.com

Myung Jin Yim
Apple Inc.
myung27@hotmail.com

Hongbin Yu
Arizona State University
yuhb@asu.edu

Zhangming Zhou
Qualcomm
zhou.zhming@gmail.com

Electrical Design & Analysis (ex RF, High-Speed Components & Systems)

Chair
Jaemin Shin
Qualcomm Technologies, Inc.
jaemins@qti.qualcomm.com

Assistant Chair
Hideki Sasaki
Rapidus Corporation
hideki.sasaki@rapidus.co.jp

Amit P. Agrawal
Microchip Technologies
amit.agrawal@amd.com

Kemal Aygun
Intel Corporation
kemal.aygun@intel.com

Wendem Beyene
Facebook
wendem@gmail.com

Eric Beyne
imec
eric.beyne@imec.be

Prem Chahal
Michigan State University
chahal@msu.edu

Harrison Chang
ASE
harrison_chang@aseglobal.com

Zhaoqing Chen
IBM Corporation
zhaoqing@us.ibm.com

Charles Nan-Cheng Chen
Shanghai Jiao Tong University
hi2018.charles@gmail.com

Craig Gaw
NXP Semiconductor
c.a.gaw@ieee.org

Xiaoxiong (Kevin) Gu
Metawave
xgu@ieee.org

Rockwell Hsu
Cisco Systems, Inc.
rohsu@cisco.com

Lianjun Liu
NXP Semiconductor, Inc.
lianjun.liu@NXP.com

Sungwook Moon
Samsung Electronics
sw2013.moon@samsung.com

Rajen M Murugan
Texas Instruments
r-murugan@ti.com

Ivan Ndip
Fraunhofer IZM/Brandenburg University of Technology (BTU)
ivan.ndip@izm.fraunhofer.de

P. Markondeya Raj
Florida International University
mpulugur@fiu.edu

Li-Cheng Shen
Universal Scientific Industrial Co. Ltd. (USI)
li-cheng_shen@usiglobal.com

Srikrishna Sitaraman
Marvell Technology
srikrishna.sitaraman@gmail.com

Xiao Sun
IMEC
xiao.sun@imec.be

Manos M. Tentzeris
Georgia Institute of Technology
etentze@ece.gatech.edu

Chuei-Tang Wang
Taiwan Semiconductor Manufacturing Company (TSMC)
ctwang10492@hotmail.com

Maciej Wojnowski
Infineon Technologies AG
maciej.wojnowski@infineon.com

Yong-Kyu Yoon
University of Florida
ykyoon@ece.ufl.edu

Thermal/Mechanical Simulation & Characterization

Chair
Karsten Meier
TU Dresden
karsten.meier@tu-dresden.de

Assistant Chair
Rui Chen
Eastern Michigan University
rchen7@emich.edu

Christopher J. Bailey
Arizona State University
christopher.j.bailey@asu.edu

Liangbiao Chen
On Semiconductor
bill.chen@onsemi.com

Kuo-Ning Chiang
National Tsinghua University / Department of Power Mechanical Engineering
knchiang@pme.nthu.edu.tw

Ercan (Eric) Dede
Toyota Research Institute of North America
eric.dede@toyota.com

Xuejun Fan
Lamar University
xuejun.fan@lamar.edu

Przemyslaw Gromala
Robert Bosch GmbH
pgromala@ieee.org

Pradeep Lall
Auburn University
lall@auburn.edu

Chang-Chun Lee
National Tsinghua University (NTHU)
cclee@pme.nthu.edu.tw

Guangxu Li
Texas Instruments
guangxu3559@gmail.com

Ruiyang Liu
TeraDAR Inc.
ruiyang.liu9@gmail.com

Yong Liu
ON Semiconductor
yong.liu@onsemi.com

Erdogan Madenci
University of Arizona
madenci@email.arizona.edu

Tony Mak
Wentworth Institute of Technology
t.mak@ieee.org

Patrick McCluskey
University of Maryland
mcclupa@umd.edu

Jiamin Ni
IBM
nijiamin8910@gmail.com

Erkan Oterkus
University of Strathclyde
erkan.oterkus@strath.ac.uk

Suresh K. Sitaraman
Georgia Institute of Technology
suresh.sitaraman@me.gatech.edu

Wei Wang
Qualcomm Technologies, Inc.
weiwang.cu@gmail.com

Zhi Yang
Groq
zyang@groq.com

Ning Ye
Western Digital
ning.ye@wdc.com

G. Q. (Kouchi) Zhang
Delft University of Technology (TUD)
g.q.zhang@tudelft.nl

Xiaowu Zhang
Institute of Microelectronics (IME)
xiaowu@ime.a-star.edu.sg

Tieyu Zheng
Microsoft Corporation
tizheng@microsoft.com

Jiantao Zheng
Hisilicon
zheng.jiantao@hisilicon.com

Photonics

Chair
Takaaki Ishigure
Keio University
ishigure@appi.keio.ac.jp

Assistant Chair
Christopher Striemer
AIM Photonics
cstriemer@gmail.com

Ankur Agrawal
Intel Corporation
ankur.agrawal@intel.com

Stephane Bernabe
CEA Leti
stephane.bernabe@cea.fr

Surya Bhattacharya
IME
bhattass@ime.a-star.edu.sg

Christopher Bower
X-Display Company, Inc.
chris@xdisplay.com

Nicolas Boyer
Ciena
nboyer@ciena.com

Lars Brusberg
Corning
brusbergl@corning.com

Mark Earnshaw
Nokia
mark.earnshaw@nokia-bell-labs.com

Gordon Elger
Technische Hochschule Ingolstadt
gordon.elger@thi.de

Z. Rena Huang
Rensselaer Polytechnic Institute
zrhuang@ecse.rpi.edu

Ajey Jacob
University of Southern California (USC)
ajey@isi.edu

Aditya Jain
Lightmatter
ajain@lightmatter.co

Soon Jang
ficonTEC USA
soon.jang@ficontec.com

Harry G. Kellzi
Micropac Industries
harrykellzi@micropac.com

Hideyuki Nasu
Furukawa Electric
hideyuki.nasu@furukawaelectric.com

Richard Pitwon
Resolute Photonics Ltd
richard.pitwon@resolutephotonics.com

Vivek Raghuraman
Broadcom Corporation
vivek.raghuraman@gmail.com

Dadi Setiadi
Lightelligence
dadi.setiadi@lightelligence.ai

Hiren Thacker
Cisco Systems
hithacke@cisco.com

Masao Tokunari
IBM Corporation
tokunari@jp.ibm.com

Stefan Weiss
II-VI Laser Enterprise GmbH
stefan.weiss@II-VI.com

Yutong Wu
TSMC
ytwux@tsmc.com

Ping Zhou
LDX Optronics, Inc.
pzhou@ldxoptronics.com

Emerging Technologies

Chair
Xinpei Cao
Henkel Corporation
xinpei.cao@henkel.com

Assistant Chair
Chukwudi Okoro
Corning
OkoroC@corning.com

Isaac Robin Abothu
Siemens Healthineers
Isaac.abothu@siemens-healthineers.com

Karlheinz Bock
TU Dresden
karlheinz.bock@tu-dresden.de

Benson Chan
Binghamton University
chanb@binghamton.edu

Vaidyanathan Chelakara
Cisco
cvaidy@cisco.com

Rabindra N. Das
MIT Lincoln Labs
rabindra.das@ll.mit.edu

Mariia Gorchichko
Applied Materials
maria.gorchichko@gmail.com

Dongming He
Qualcomm Technologies, Inc.
dhe@qti.qualcomm.com

Florian Herrault
PseudolithIC, Inc
floherrault@gmail.com

Jae-Woong Jeong
KAIST
jjeong1@kaist.ac.kr

Tengfei Jiang
University of Central Florida
tengfei.jiang@ucf.edu

Hee Seok Kim
University of Washington Tacoma
heeskim@uw.edu

Jong-Hoon Kim
Washington State University Vancouver
jh.kim@wsu.edu

Santosh Kudtarkar
Analog Devices
santosh.kudtarkar@analog.com

Kevin J. Lee
Qorvo Corporation
kevinJ.Lee@qorvo.com

Zhuo Li
Fudan University
zhuo_li@fudan.edu.cn

Yang Liu
Nokia Bell Labs
yang3d@gmail.com

Dishit Parekh
Intel
dishit.parekh@intel.com

C. S. Premachandran
GlobalFoundries
319prem@gmail.com

Jintang Shang
Southeast University
shangjintang@hotmail.com

Ran Tao
National Institute of Standards and Technology
ran.tao@nist.gov

W. Hong Yeo
Georgia Institute of Technology
whyeo@gatech.edu

Hongqing Zhang
IBM Corporation
zhangh@us.ibm.com

Professional Development Courses

Chair
Kitty Pearsall
Capstan Technologies
kitty.pearsall@gmail.com

Assistant Chair
Jeffrey Suhling
Auburn University
jsuhling@auburn.edu

PROFESSIONAL DEVELOPMENT COURSES

Tuesday, May 27, 2025

Kitty Pearsall, Chair
Capstan Technologies
kitty.pearsall@gmail.com
+1-512-845-3287

Jeff Suhling, Assistant Chair
Auburn University
jsuhling@auburn.edu

MORNING COURSES
8:00 a.m. – 12:00 Noon

1. HIGH RELIABILITY SOLDERING IN SEMICONDUCTOR PACKAGING

Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech

Course Description:

Semiconductor soldering is much more delicate and is critical for reliability of devices. The course covers the critical parameters governing the reliability for soldering in semiconductor packaging. The reliability discussed includes parameters affecting the intermetallic compounds (IMC), voiding, electromigration, low-temperature soldering, high-temperature soldering, and electrochemical migration under a variety of material combinations. The failure modes are discussed in detail, with preferred choices of materials and designs recommended.

Course Outline:

1. IMC - Effect of Cu Pad Grain Size on IMC
2. IMC - Interaction of Cu and Ni
3. IMC - Effect of Base Metal Co-P on IMC
4. Voiding - Effect of Solder Form on Voiding
5. Voiding - Effect of Joint Height, Temperature, Electrical, Mechanical on Kirkendall Voiding
6. Voiding - Effect of Cu Structure on Kirkendall Voids
7. Electrochemical Migration (ECM)
8. Electromigration
9. LTS - Bi-Rich Whisker Growth
10. LTS - TCT Reliability of LTS
11. LTS - Collapse of LTS
12. LTS - Deposition, Hot Tear, Bi Stratification of LTS
13. LTS - Hot Tear of Homogeneous LTS BiSn - Effect of Profile
14. LTS - Drop Test of LTS
15. HTS - TLPB (Transient Liquid Phase Bonding)

IMPORTANT NOTICE

Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

Who Should Attend:

Anyone who cares about achieving high reliability solder joints for semiconductor packaging and wants to know how to achieve it should take this course

2. PHOTONIC TECHNOLOGIES FOR COMMUNICATION, SENSING, AND DISPLAYS

Course Leader: Torsten Wipiejewski – Huawei Technologies

Course Description:

This course will provide an overview on the various photonic technologies that enable optical communication, optical sensing, and modern display applications. These applications are key for the information and communication technology of today and pave the way to the future. High-speed optical communication from board level in data centers to long haul transmission requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of various types, high-speed optical modulators and photodetectors as well as integration schemes such as photonic integrated circuits PICs and packaging aspects. Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitates the usage by end-users without specific medical knowledge. Optical sensor packaging should provide high accuracy solutions at low cost. Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro-LEDs. In particular, micro-LEDs for large size displays require novel assembly technologies.

Course Outline:

1. Fundamental Properties of Photonic Components
2. Light Sources (LEDs, Laser Diodes, VCSELs)
3. Transmitter and Receiver Components in Optical Communication Systems (Lasers, Modulators, Photodetectors)
4. Optical Modules, Monolithic and Hybrid Integration, Packaging.
5. Optical Sensing Elements and Applications (Spectrometers, Light Sources, Photoacoustic Sensors, Frequency Combs)
6. Display Technologies: Liquid Crystal Displays (LCD), Organic Light Emitting Diode Displays (OLED), Quantum Dot Emissive Layers, Micro-LED Displays Made by Chiplet Mass Transfer, and Bonding
7. Summary and Outlook

Who Should Attend:

The course addresses engineers, scientists, and students who would like to get a general overview on various photonics technologies used in today's products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are as well as potential technology breakthroughs.

3. FROM WAFER TO PANEL LEVEL PACKAGING

Course Leaders: Tanja Braun and Piotr Mackowiak – Fraunhofer IZM

Course Description:

Wafer and Panel Level Packaging are two of the dominating trends in microelectronics packaging. Both approaches with different flavors as RDL-last face-up or face-down have reached maturity and are introduced in high volume manufacturing. Main driver for moving from wafer to panel level packaging is of course lowering the packaging cost. More packages can be processed in parallel, and rectangular panel formats have a much better area utilization than circular wafers. With the advent of chiplet technology and the application to large body size packages e.g. HPC modules Panel Level Packaging is actually gaining momentum as an option for lower cost and high-density packaging. The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

Course Outline:

1. Introduction to Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-out Wafer Level: Material, Processes, Applications
4. Introduction and Definition Panel Level Packaging (PLP)
5. Fan-out Panel Level Packaging: Technologies, Challenges & Opportunities

Who Should Attend:

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging. Engineers and managers are welcome as detailed technology descriptions as well as market trends, applications and cost modelling are presented.

4. ELIMINATING FAILURE MECHANISMS IN ADVANCED PACKAGES

Course Leader: Darvin Edwards – Edwards Enterprises

Course Description:

Primary reliability failure mechanisms that plague semiconductor packages will be detailed along with solutions to enable faster qualification. The reliability of new package technologies such as heterogeneous package integration and chiplets will be emphasized, as well as an overview of reliability issues in more traditional packages. Topics highlighted include reliability of Direct Cu Bonding (DCB), high density interconnect (HDI) reliability, TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced interlevel dielectric (ILD) damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, the impact of aging on reliability performance and many more. Primary failure analysis techniques will be described. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on the key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. A primary goal is to give the student an intuitive understanding of the interaction between the various trade-offs and to provide the knowledge of the methodologies and tools needed to drive early evaluation of these reliability risks.

Course Outline:

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques
4. FC-BGA Package Failure Mechanisms
5. WLCSP Package Failure Mechanisms
6. Embedded Die & Fan-Out WLP/PLP Failure Mechanisms
7. TSV Failure Mechanisms
8. High Density Interconnection Reliability
9. Direct Bond Interconnect Reliability and Testing
10. Chiplet Challenges
11. Materials, Modeling, Design Rules and Reliability
12. Summary

Who Should Attend:

This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

5. INTRODUCTION TO AND ADVANCES IN 2.3D FAN-OUT WAFER LEVEL PACKAGING (FO-WLP)

Course Leader: Beth Keser – Zero ASIC

Course Description:

Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 20 years and have been in high volume manufacturing for over 16 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. After scale-up and high-volume manufacture of simple single-chip Fan-Out Wafer Level Packaging (FO-WLP) solutions by companies like Qualcomm and Infineon, now many premier semiconductor companies and OEMs have adopted Advanced Fan-Out structures including Apple, AMD, MediaTek, and HiSilicon. These companies are leveraging foundry technologies like InFO offered by TSMC as well as OSAT solutions from ASE, Amkor, SPIL, PTI, and DECA.

The introductory portion of this course will cover the advantages of FO-WLP, potential application spaces; package structures available in the industry; materials, equipment and process challenges; and reliability. The advanced topics will cover potential application spaces, advanced package structures available in the industry, adopting 2.3D chips first and chips last fan-out technology for chiplets, technology roadmaps, and benchmarking.

Course Outline:

1. Definitions and Advantages
2. Applications
3. Early Package Structures
4. Materials
5. Equipment
6. Design Rules and Reliability
7. Advanced Applications Including Chiplets
8. Package Structures Including Advanced FO Technologies
9. Technology Roadmap
10. Panel Challenges
11. Benchmarking

Who Should Attend:

Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Suppliers who are interested in supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

6. WAFER-TO-WAFER AND DIE-TO-WAFER HYBRID BONDING FOR ADVANCED INTERCONNECTS

Course Leader: Viorel Dragoi – EV Group E. Thallner GmbH

Course Description:

This course addresses fundamental and practical aspects of low temperature fusion and hybrid bonding, aiming to provide a good understanding of the current status and potential of this technology to provide manufacturing solutions for current and future applications. The course starts with a brief overview of all wafer bonding processes currently in use. A detailed explanation of the working principles of low temperature fusion and hybrid bonding is presented. Aspects related to material specifications and surface preparation are reviewed. Wafer-to-wafer alignment concepts are further introduced, with emphasis on face-to-face alignment. An overlay model is introduced and its benefits of its use are illustrated with experimental results. Aspects of implementing advanced process control methods are discussed, with an example on bond wave monitoring and control.

The concept of die-to-wafer bonding is introduced as a heterogeneous integration technology for chiplets-based applications. The different process flows available are reviewed. Some important aspects specific to die-to-wafer bonding are discussed, with emphasis on dies preparation and specific requirements of the various process flows. Experimental results are used for illustration of this technology's capabilities. This course concludes with a brief overview of the current and future challenges of wafer bonding.

Course Outline:

1. Introduction: Wafer Bonding Processes Short Overview (Principles, Basic Conditions)
2. Short Overview of the Wafer Bonding Process Variables
3. Low Temperature Fusion Bonding: Description, Specifications, Surface Preparation and Activation, Bonding Process
4. Low Temperature Hybrid Bonding: Description, Specifications, Surface Preparation, Bonding Process
5. Wafer-to-wafer Alignment: General Principles (Methods, Errors), SmartView Alignment Introduction, Overlay and Distortion
6. Advanced Process Control: Using Numerical Simulation and Data Analysis
7. Advanced Bond Wave Monitoring and Control
8. Short Overview of Wafer Bonding - Specific Metrology: Defects, Bond Strength

9. Die-to-wafer Bonding: Introduction of the Concept and Process Flows
10. Die-to-wafer: Specific Process Features Compared to Wafer-to-wafer Bonding (Dies Preparation, Alignment, and Metrology)
11. Summary: Short Overview of Wafer Bonding Current and Future Challenges

Who Should Attend:
The course is addressed to engineers involved in heterogeneous integration technology development who are willing to understand the status of wafer bonding technology and its applications potential. Principles and concepts are presented and explained together with more advanced topics. No prior experience in wafer-to-wafer or die-to-wafer bonding is required.

7. FUNDAMENTALS OF FABRICATION PROCESSES AND RF DESIGN OF ADVANCED PACKAGES INCLUDING FAN-OUT, CHIPLETS, GLASS AND POLYMER INTERPOSER

Course Leaders: Ivan Ndip – Brandenburg University of Technology/Fraunhofer IZM and Markus Wöhrmann – Fraunhofer IZM

Course Description:
Advanced packaging technologies such as fan-out wafer and panel level packages (FO-WLPs, FO-PLPs), interposers (e.g., glass interposers with TGVs, polymer interposers) and chip-embedding packages (e.g., PCB embedding) play a key role in heterogeneous integration and enable the development of system in package (SiP) modules, antenna in/on-package (AiP/AoP) and chiplet based systems. The packaging materials, fabrication processes and RF performance of these packages contribute significantly to the cost, performance and reliability of the entire system.

The main objective of this course is to provide a thorough overview of packaging materials, fundamentals of fabrication processes and basic RF design of advanced packages (e.g., FO-WLPs, FO-PLPs, glass and polymer interposers, SiP and AiP/AoP) for a wide range of applications. Furthermore, an introduction to chiplet design and heterogeneous integration, considering interconnects for chiplet communication and UCIe, will be given. The applications driving advanced packages such 5G, 6G communication, radar sensing, high-performance computing (HPC) and AI in various industries will also be extensively discussed.

Course Outline:
1. Introduction, Basic Definitions and Explanations of Key Terminologies Related to Advanced Packages, RF Design, Chiplets, and Heterogeneous Integration
2. Applications Driving Advanced Packages such as 5G, 6G Communication, Radar Sensing, HPC, and AI in Various Industries
3. Overview of Different Types of Advanced Packages, Current Trends, and Future Directions
4. Challenges and Key Requirements of Advanced Packages for RF Applications
5. Fundamentals of Packaging Materials and Fabrication Processes of FO-WLPs/FO-PLPs, Interposers (Glass, Organic), and AiP/AoP
6. Role of Electrical Parameters (Dk and Df) of Materials in RF Packaging and Methods for Measurement-Based Extraction of Dk and Df of Different Packaging Materials
7. Fundamentals of RF Design of Building Blocks of FO-WLPs/FO-PLPs, Interposers (Glass, Organic), and AiP/AoP
8. Introduction to Chiplet Design and Heterogeneous Integration, Considering Interconnects for Lateral Chiplet Communication and UCIe
9. Examples of Advanced Packages Fabricated at Fraunhofer IZM

Who Should Attend:
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication, and/or system-integration of electronic packages for emerging applications (e.g., 5G, 6G, mmWave radar sensors) should attend.

8. DESIGN OF RELIABLE DATA CENTER COOLING SYSTEMS

Course Leaders: Patrick McCluskey and Damena Agonafer – University of Maryland

Course Description:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics. This course will emphasize approaches to integrated thermal packaging that address performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g. organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and in the techniques for their reliability assessment.

Course Outline:
1. State of the Art Data Center Cooling
2. Single Phase Liquid and Hybrid Cooling Approaches
3. Thermal Modeling
4. Reliability and Availability Modeling
5. Software Tools for Modeling
6. Examples of Leading-Edge Cooling Solutions

Who Should Attend:
Data Center Designers, HVAC Engineers, Electronic Packaging Engineers and Managers interested in addressing key challenges to the growth of data centers.

AFTERNOON COURSES
1:30 p.m. – 5:30 p.m.

9. 3D PACKAGING FAILURE ANALYSIS – FAILURE MECHANISMS AND ANALYTICAL TOOLS

Course Leader: Deepak Goyal – Independent Consultant

Course Description:
Heterogeneous Integration (HI) of disparate computing and communications functions is a key enabler of performance in micro-electronic systems. HI is crucially enabled by advanced packaging since packages are an optimal HI platform. This technical course will provide an overview of the failure modes and mechanisms observed in 2.5D/3D packages. A brief introduction to the methodology of failure analysis of these packages will be described. The focus of the course will be on package failure mechanisms highlighted by case studies and on analytical tools and techniques currently used and the future direction for the tools and techniques required for successful and timely failure analysis of 3D package technologies. A discussion on the strategies for use of these techniques and a flow chart for failure analysis will be included.

Course Outline:
1. 2.5D/3D Package Technology – Trends, Drivers & Challenges
2. Failure Analysis Challenges Offered by 3D Package Technology Roadmap
3. Introduction to the Methodology of Failure Analysis of 3D Packages
4. Current Analytical Capabilities for Package Fault Isolation and Failure Analysis

5. Strategies to Use These Techniques to Identify Failures and Understand Failure Mechanisms
6. Analytical Capabilities to Support Next Generation 3D Packaging Technologies
7. Typical Failure Analysis Flow Charts for Opens and Shorts.
8. Failure Modes/mechanisms Including Chip/package Interactions, 1st/2nd Level Interconnections and Package/board Substrates.
9. Failure Analysis Case Studies.

Who Should Attend:
Engineers and technical managers who are involved in package technology development, assembly manufacturing, reliability assessment of packages and failure analysis will benefit from this course.

10. DIAMOND FOR HETEROGENEOUS INTEGRATION

Course Leader: Joana Mendes – University of Aveiro

Course Description:
Enhanced power density in 3D/2.5D integrated systems has led to a significant increase in the complexity of thermal management. In fact, thermal issues systems are increasingly moving to the forefront as a major challenge limiting the overall electrical performance and reliability of components in 3D/2.5D integrated systems. The thermal integrity of future heterogeneously integrated systems will not be achieved unless problems related to material properties are addressed. This course will discuss the potential of integrating synthetic diamond in complex SiPs to improve heat extraction and increase reliability. The methods for fabricating synthetic diamonds will be described and their pros and cons discussed. Different strategies that can be employed to integrate diamond in the concept of 3D/2.5D integration will be proposed and a critical assessment of the expected technical challenges and possible solutions will be made. Recent research work and breakthroughs from both industry and academia will be presented. Finally, the recent trend of gemstone market saturation and the impact on the cost of synthetic diamond will be discussed. NOTE: a video of a much-shorter version or segment is available on IEEE.tv (https://r6.ieee.org/scv-eps/?p=3189)

Course Outline:
1. Potential of Synthetic Diamond for Thermal Management Applications
2. Methods for Fabricating Synthetic Diamond, Advantages and Limitations
3. Integrating Synthetic Diamond at Different Levels in a SiP
4. Diamond for Thermal Management: Successful Examples
5. GaN HEMTS: Diamond Substrates and Diamond Capping
6. Semiconductor Disk Lasers: Diamond Sub-mounts and Heat Spreaders
7. High Power Components: Diamond Boards and Die-carriers
8. Bonding of Diamond and Non-diamond Wafers
9. Microfluidics Using Diamond
10. Current Issues and Guidelines for Solutions
11. Foreseen Synthetic Diamond Market Trends

Who Should Attend:
Researchers and practitioners looking for thermal management solutions for heterogeneously integrated packaging should attend. Managers considering the use of alternative approaches to thermal problems will also benefit from attending.

11. CHIPLET, HETEROGENEOUS INTEGRATION, AND CO-PACKAGED OPTICS

Course Leader: John Lau – Unimicron

Course Description:
Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components with different sizes and functions, and from different fabless design houses and foundries into a system or subsystem on a common package substrate. Co-packaged optics (CPO) are heterogeneous integration of the optical engine which consists of photonic ICs (PIC) and the electrical engine (EE) which consists of the electronic ICs (EIC) as well as the switch ASIC (application-specific integrated circuitry). The advantages of CPO are: (a) to reduce the length of the electrical interface between the OE/EE (or PIC/EIC) and the ASIC, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging and CPO, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the introduction, recent advances, and trends in chiplet, HI, and CPO will be presented.

Course Outline:
1. System on Chip (SOC)
2. The Origin of Chiplets
3. Chiplet Design and HI Packaging (1. Partition, 2. Split)
4. Communication Between Chiplets (EMIB, UCIe, Bridge Embedded in Fan-Out EMC)
5. Chiplet Design and HI Packaging - Multiple System and HI
6. Potential R&D Topics in Chiplet Design and HI Packaging
7. Trends in Chiplet Design and HI Packaging
8. Silicon Photonic
9. Data Centers and Optical Transceivers
10. Optical Engine (OE) and Electrical Engine (EE)
11. OBO (On-Board Optics), NBO (Near-Board Optics), and CPO (Co-Packaged Optics)
12. 3D HI of PIC and EIC
13. 3D HI of ASIC Switch, PIC and EIC w/o Bridges
14. 3D HI of GPU, HBM, Switch, PIC, EIC (Driven by AI)
15. HI of ASIC Switch, PIC and EIC on Glass Substrate
16. Potential R&D Topics and Trends in Co-Packaged Optics

Who Should Attend:
If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. Each attendee will receive more than 300 pages of lecture notes.

12. ANALYSIS OF FRACTURE AND DELAMINATION IN MICROELECTRONIC PACKAGES

Course Leader: Andrew Tay – National University of Singapore

Course Description:
The main objective of this course is to provide a fundamental understanding as well as proven techniques of applying the fracture mechanics methodology to predicting fracture and delamination in microelectronic packages. The mechanism of popcorn cracking failure will be described and analyzed. Simulation of heat transfer and moisture diffusion processes occurring during package qualification and reflow will be described. An introduction to the fundamentals of interfacial fracture mechanics will be given together with descriptions of some numerical methods for calculating fracture mechanics parameters. Experiments which verify the methodology for predicting delamination in packages will be described followed by some case studies.

Course Outline:
1. Hygrothermal Stresses in Microelectronics Packages
2. Finite Element Analysis and Stress Singularities
3. Fundamentals of Fracture Mechanics Methodology
4. Determination of Fracture Mechanics Parameters
5. Measurement of Fracture Toughness
6. Experimental Verification of the Fracture Mechanics Methodology
7. Case Studies on Delamination of Pad-encapsulant Interfaces, Die-attach Layers and On-chip Interconnect Structures (BEOL)
8. Cohesive Zone Modelling of Delamination and Case Studies

Who Should Attend:
This course is designed for packaging design engineers who perform reliability analysis of microelectronics and photonics packages. Knowledge of finite element analysis is an advantage but not essential.

13. ADVANCED FAN-OUT DEVELOPMENTS AND APPLICATIONS

Course Leaders: John Hunt and Jan Vardaman – TechSearch International, Inc.

Course Description:
Fan-out wafer-level packaging (FO-WLP) has evolved from a low-cost packaging option for automotive and mobile applications to a high-performance computing packaging solution. Both chip-first and chip-last solutions have been adopted and are expanding in complexity to serve a range of applications including AI training and inferencing, replacing silicon with an organic redistribution layer (RDL) as the interposer. The potential for packaging for RF and photonics is also described. The course provides a brief overview of the various fan-out packages, a history of their evolution, and discussion of the current structures and reasons for adoption in each application. Differences between the three basic processes flows: Chip First Die Down, Chip First Die Up, and Chip Last are explained with examples of each structure. Bridge solutions are described, including process flows, advantages, and applications. The course also discusses the move to large panels for cost-reduction and discusses both the potential advantages and challenges. Production examples and process flows are included.

Course Outline:
1. Overview: Drivers for Fan Out
2. Basic Low-density Fan Out
3. 3D Fan Out Structures
4. High Density Die to Die Fan Out
5. Fan Out Embedded Bridge Technology
6. Fan Out System in Package
7. Antenna in Package
8. Fan Out Silicon Photonics Integration
9. Fan Out Memory Packaging
10. Panel Fan Out

Who Should Attend:
Anyone interested in understanding FO-WLP and the differences between the various FO-WLP structures, individuals interested in understanding the advantages of the various types of fan-out for different applications, and engineers and managers who would benefit from an understanding of the landscape of package options, advantages, and alternatives.

14. FLIP CHIP TECHNOLOGIES

Course Leader: Shengmin Wen – TATA Electronics

Course Objectives:
Advanced packaging, such as CSP, FCBGA, 2.5D/3D, HBM packaging, heterogeneous packaging with multiple dies and multiple Si nodes, embedded die packaging, certain wafer level package or panel level packaging, is based on flip chip technologies. For high-speed, high-performance applications such as AI-targeted design, flip chip technology is a must. Even some traditional packaging types such as QFN begin to use flip chip technology. Industry-wise in terms of total annual revenue Flip chip packaging has grown steadily and already passed wire bond-based packaging.

This course will cover the fundamentals of flip chip assembly technologies, including major assembly processes, wafer bumping technologies, substrate types and critical BOM selection, design rules, and reliability modeling/evaluation.

Two major assembly processes, their related equipment, materials, design rules, and design practices are covered in detail. Examples are presented to demonstrate the versatile flip chip integrations, including single-die, monolithic multi-die, multi-level multi-die, as well as multi-form mixed interconnection that uses both wire bond / flip chip integration.

In-depth discussions include chip package interaction (CPI), package warpage control, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, Si die floor plan optimization, design rules, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their future projects.

Various bumping technologies that are used in today's flip chip assembly are also briefly introduced, i.e., lead-free solder bumping and highly customized Cu-Pillar bumping. The course will also cover various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

A group exercise at the end of the class is planned to serve as an in-class capstone project, ensuring that the students walk away with an in-depth understanding of the flip chip assembly technologies, and are ready to apply the knowledge to their real-world packaging designs and projects.

Course Outline:
1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Flip Chip Substrate Technologies
5. Underfill, Package Warpage Control, and Yield Detractors
6. Failure Modes, Examples, Modeling and Reliability Life Assessment
7. Flip Chip Si Package Co-Design on Various Types (BOT, BOP, AI Type) and Examples
8. Variations: Wafer Level CSP, Wafer Level Fan-Out, Panel Level Packaging, Hybrid Bonding
9. Bumping Process, Rules, and Introduction
10. Flip Chip Under-Bump Metallization and Intermetallic
11. Review and Package Selection Exercise – Group Discussions

IMPORTANT NOTICE
Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

Who Should Attend:
Anyone who wants to understand the fundamentals of flip chip packaging technology are encouraged to take this highly condensed and yet knowledge content fully covered course. These include graduate students who look for a packaging engineering career, engineers who are to take advanced package projects, project managers who want to have an in-depth technical understanding every step of the way, and managers who want to expand their understanding of key aspects of flip chip technologies to flawlessly adopt to a company's product roadmap. This course may help materials and equipment vendors to understand the applications.

15. DESIGN-ON-SIMULATION FOR ADVANCED PACKAGING: WARPAGE MANAGEMENT, RELIABILITY AND LIFE PREDICTION

Course Leaders: Kuo-Ning Chiang – National Tsing Hua University and Xuejun Fan – Lamar University

Course Description:
The electronic packaging community has widely used Design-on-Simulation (DoS) methodology for designing new packaging structures in terms of warpage management, reliability, and life prediction. Artificial intelligence (AI) / machine learning (ML) approaches can be combined with DoS for better accuracy and efficiency. This course aims to illustrate the fundamentals of physics associated with different failure mechanisms, in particular, the warpage management, and the solution methodology and procedure for large database generation, and AI training performance of different machine learning algorithms. This course will also describe the warpage mitigation solutions, as well as how to combine AI and finite element simulation to estimate the reliability life and obtain the best structure combination of each packaging component using wafer-level packages as demonstrations.

Course Outline:
1. Introduction to Advanced Packaging
2. Root Causes of Warpage and Mechanics
3. Warpage Management

4. Local-global and Mesh Size Control Technology, Finite Element Analysis and Simulation
5. AI-assisted Design-on-simulation Methodology
6. AI solvers
7. Case study: Solder Joint Reliability Life Cycle Prediction Empirical Equations

Who Should Attend:
This course is intended for technical managers and staff members, reliability engineers, scientific researchers, and graduate students who are involved in thermal/mechanical modeling, package design, material selection, qualification and reliability assessment of chip-package interaction, package, and package/board interaction.

16. CURRENT AND FUTURE CHALLENGES AND SOLUTIONS IN AI & HPC SYSTEM AND THERMAL MANAGEMENT

Course Leader: Gamal Refai-Ahmed – AMD

Course Description:
Are you ready to dive into the forefront of AI and HPC system thermal management? This dynamic and interactive course is designed to equip you with cutting-edge knowledge and practical skills to tackle the current and future challenges in thermal management and packaging. Dr. Refai Ahmed, a distinguished technical executive with over two decades of industry experience at giants like AMD, GE, and Cisco, brings unparalleled expertise to this course. His groundbreaking work in thermal management, silicon and power architecture, and advanced packaging technologies, supported by numerous patents and publications, sets the foundation for this comprehensive learning experience.

Key Takeaways:

- A comprehensive understanding of current and future challenges in thermal management and packaging.
- Exposure to innovative solutions and state-of-the-art technologies.
- Practical insights that enhance daily engineering practices and drive industry advancements.

Course Outline:

1. Introduction
2. Thermal & Packaging Roadmap and Challenges
3. Next-Generation Thermal Management Architecture
4. First-Line and Second-Line Cooling Solutions
5. Advanced Cooling Techniques
6. Dynamic Discussions and Hands-On Experience

Who Should Attend:
This course promises to be highly interactive and practical, drawing on industrial developments from the first principles of engineering and showcasing advanced thermal-mechanical solutions. Join us to explore the forefront of AI and HPC system thermal management and gain knowledge that will propel your career forward. Whether you're looking to deepen your expertise or stay ahead.

IMPORTANT NOTICE

Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.
See page 32 for registration information

Program Sessions: Wednesday, May 28, 9:30 a.m. - 12:35 p.m.

Session 1: Processing and Packaging Articles for 3D Integration	Session 2: Co-Packaged Optics	Session 3: Hybrid Bonding Materials and Processing for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Photonics**	**Committee:** **Materials & Processing**
Session Co-Chairs **Subhash L. Shinde** **Notre Dame University** **Email: sshinde@nd.edu** **Peng Su** **Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs** **Soon Jang** **ficonTEC USA** **Email: soon.jang@ficontec.com** **Hiren Thacker** **Cisco Systems, Inc.** **Email: hithacke@cisco.com**	**Session Co-Chairs** **Vidya Jayaram** **Intel Corporation** **Email: vidya.jayaram@intel.com** **Hongbin Yu** **Arizona State University** **Email: Hongbin.Yu@asu.edu**
1. 9:30 AM - SoW-X: A Novel System-on-Wafer Technology for Next Generation AI Server Application Po-Chang Shih, An-Jhih Su, Tze-Chiang Huang, King-Ho Tam – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Heterogeneous Integration of Fiber-Based Co-Packaged Optics With EMIB Technology: Assembly, Performance, and Reliability*** Kumar Abhishek Singh, Ziyin Lin, Peter Williams, Darren Vance, Joel Wright, Bilas Chowdhury, Todd Coon, Shahin Mani – Intel Corporation	***1. 9:30 AM - Morphological Microstructure Characterization and Optimization of Nanocrystalline Copper Deposition for Fine-Pitch Hybrid Bonding Cu/SiO2 at Low Temperature.*** Mathieu Loyer, Emilie Deloffre – ST Microelectronics; Maria-Luisa Calvo-Munoz, Marie Maubert, Mathilde Gottardi, Pierre-Emile Philip, Gilles Romero – CEA-LETI
2. 9:50 AM - Face-Down Bonding and Heterogeneous Chiplet Integration by Using Bumpless Chip-on-Wafer (COW) With Waffle Wafer Technology Yoshiaki Satake, Tatsuya Funaki, Takayuki Ohba – Institute of Science Tokyo; Wataru Doi – Murata Manufacturing Co., Ltd.; Shogo Okita, Hajime Kato – Panasonic Connect Co., Ltd.	***2. 9:50 AM - 6.4Tbps, 224Gbps/Lane Co-Packaged Optical Engines With Fine Pitch Through-Package Interconnects: Powering AI/ML and Next-Gen Data Centers*** BG Sajay, Jia Qi Wu, Rathin Mandal, Sandra San, Surya Bhattacharya – Institute of Microelectronics A*STAR; Li Xin, Jason Tsung-Yang Liow – Rain Tree Photonics Pte. Ltd.	***2. 9:50 AM - Wafer-to-Wafer Bonding With Ultralow Thermal Resistance and High Bonding Energy*** Wenhao (Eric) Li, Feras Eid, Andrey Vyatskikh, Richard Vreeland, William Brezinski, Christopher Jezewski, Michael Njuki, Rajiv Mongia – Intel Corporation
3. 10:10 AM - Electrical Properties and Reliability of Back-Side Redistribution Layers Based on Inorganic Dielectrics in 3D Stacked Memory Packages Jongyeon Kim, Jaecheol Shim, Sungkyu Kim, Seungchul Han, Hoyoung Son, Kangwook Lee – SK hynix Inc.	***3. 10:10 AM - Flip-Chip Photonic-Electronic Integration Platform for Co-Packaged Optics Using a Glass Substrate With Vertically-Coupled Beam Expanding Lens*** Yasutaka Mizuno, Kunio Kobayashi, Shingo Nakamura, Masaki Migita, Hajime Arao, Tetsuya Nakanishi, Hiroshi Uemura, Keiji Tanaka – Sumitomo Electric Industries, Ltd.	***3. 10:10 AM - Novel Polymer for Hybrid Bonding With Precise Tunable Crosslink Density*** Ryo Sugano, Shintaro Nagayama, Tetsuya Ogawa, Hiroyoshi Deguchi, Eisaku Ishikawa – Resonac Corporation
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - A Novel 3D Heterogeneous Integration Using 2 µm Bond Pitch Die-to-Wafer Hybrid Cu Bonding and Wafer Reconstruction Process Pilkyu Kang, Jaejin Lee, Moonkeun Kim, Eunmi Kim, Kyu-Ha Lee, Chanmi Lee, Jaehwa Park, Minwoo Rhee – Samsung Electronics Co., Ltd.	***4. 11:15 AM - Optical and Electrical Characterization of a Compact Universal Photonic Engine*** Ming-Fa Chen, Hao-Tien Cheng, Chia-Han Tsou, Shang-Yun Hou, Ryan Lu, Kuo-Chin Hsu – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 11:15 AM - Hybrid Bonding With Particle Accommodation Using Polymer Dielectric: Design, Process and Yield Study*** Ling Xie, Ser Choong Chong, Vasarla Nagendra Sekhar – Institute of Microelectronics A*STAR; Yu Shoji, Masaya Jukei, Kota Nomura, Takenori Fujiwara, Hitoshi Araki – Toray Industries, Inc.
5. 11:35 AM - Enabling Chip-to-Wafer Hybrid Bonding Scaling to 1 µm Pitch With Optimal Power Delivery Using New Bond Via Architectures Golsa Naderi, Saurabh Chauhan,, Adel A Elsherbini, Johanna Swan, Arian Rahimi, Qiang Yu – Intel Corporation	***5. 11:35 AM - Large-Scale Glass Waveguide Circuit for Board-Level Optical Interconnects Between Faceplate and Co-Packaged Optical Transceivers*** Lars Brusberg – Corning, Inc.; Betsy Johnson, Jason Grenier, Matthew Dejneka, Chad Terwilliger – Corning Research and Development Corp.; Julian Schwietering, Christian Herbst, Henning Schroeder – Fraunhofer IZM	***5. 11:35 AM - Characterization of Self-Nanoparticulated Cu-Cu Interconnection for Low-temperature Hybrid Bonding*** Ryotaro Kawashima, Bungo Tanaka, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Hirokatsu Sakamoto – Daicel Corporation
6. 11:55 AM - Fluxless Thermocompression Bonding: Adapting to the Future Jonathan Abdilla, Martin Kainz, Benedikt Pressl, Mario Fraubaum, Chris Scanlan – Besi NL; Jaber Derakhshandeh – imec	***6. 11:55 AM - All-SMF Arrays for Co-Packaged Optics: Optimizing Cost, Complexity, and Performance*** Nandish Mehta – Nvidia Corporation	***6. 11:55 AM - AlN Gap-Fill Process by Aerosol Deposition Method for Application in 3D-IC Packaging*** Takeki Ninomiya, Takeshi Takagi, Masaaki Niwa, Tadahiro Kuroda – University of Tokyo; Masakazu Mori – Ryukoku University
7. 12:15 PM - Integration Solution for Thin D2W Hybrid Bonding for Yield and Reliability Xiaodong Chen, Guan Huei See, Patrick Lim, Prayudi Lianto, Peng Suo, Andy Yong, Santosh Kumar Rath, Xing Zhao – Applied Materials, Inc.	***7. 12:15 PM - A +21-dBm per Channel Operation of a 16-Channel CWDM ELSFP Module in Practical Air-Cooling Conditions*** Kohei Umeta, Taketsugu Sawamura, Yuki Shiroishi, Maaya Tsukamoto, Hideyuki Nasu – Furukawa Electric Co., Ltd.	***7. 12:15 PM - Effect of Grain Size on Cu-Cu Bonding Quality for Fine-Pitch Hybrid Bonding Application*** Chen-Ning Li – National Yang Ming Chiao Tung University; Chih Chen – National Yang Ming Chiao Tung University

Program Sessions: Wednesday, May 28, 9:30 a.m. - 12:35 p.m.

Session 4: Large Package Manufacturing and Panel Level Processing	Session 5: Advanced Design for Heterogeneous Integration	Session 6: AI - ML and Emerging Modeling Methods
Committee: Assembly & Manufacturing Technology	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Zia Karim** **Yield Engineering Systems** **Email: zkarim@yes.tech** **Jason Rouse** **Taiyo America, Inc.** **Email: jhrouse@taiyo-america.com**	**Session Co-Chairs** **Ivan Ndip** **Fraunhofer IZM** **Email: Ivan.Ndip@izm.fraunhofer.de** **Li-Cheng Shen** **Miniaturization Competence Center (MCC), USI** **Email: li-cheng_shen@usiglobal.com**	**Session Co-Chairs** **Pradeep Lall** **Auburn University** **Email: lall@auburn.edu** **Guangxu Li** **Texas Instruments, Inc.** **Email: guangxu_li@ti.com**
1. 9:30 AM - Package Warpage Reduction for Large CoWoS-R Packages Yu-Hsiang Hu, Kathy Yan, Chien-Hsun Lee, Jyun-Siang Peng, Hsin-Yu Chen, Pei-Hsuan Lee, Jowett Lee, P Chen – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Enabling 20 Tb/s/mm Die-to-Die Bandwidth Density With Advanced Packaging Technologies*** Zhiguo Qian, Kemal Aygun – Intel Corporation	***1. 9:30 AM - NAND Package Warpage Prediction and Design With Tolerance Through Machine Learning*** Min Lin, Chaolun Zheng, Yuhang Yang, Ning Ye, Bo Yang – Western Digital Corporation
2. 9:50 AM - Process Development and Reliability Investigation of 120 mm x 120 mm Large 2.5D Package With Low Melting Temperature Solder Kazue Hirano, Dongchul Kang, Masaki Takahashi, Motoo Aoyama, Yuji Inui, Sadaaki Katoh – Resonac Corporation	***2. 9:50 AM - Novel Organic Interposer Design for Automotive Chiplet 2.5D Package With UCIe Advanced*** Hiroki Shibuya, Shuuichi Kariyazaki, Tatsuaki Tsukuda – Renesas Electronics Corporation	***2. 9:50 AM - Compact Models for Nonlinear Thermo-Mechanical Simulations of Chiplets in Automotive*** Mike Manuel Feuchter, Hanna Baumgartl, Martin Hanke – CADFEM GmbH; Przemyslaw Gromala, Bragadesh Srivatsan – Robert Bosch GmbH; Ghanshyam Gadhiya, Sven Rzepka – Fraunhofer ENAS
3. 10:10 AM - New Silicon Capacitor Solutions With Over 1mm -Thick Core Based Embedded Substrate for Extremely Large Package Platform Kyojin Hwang, Woobin Jung, Sunghawn Bae, Kisu Joo, Junso Pak, Heeseok Lee – Samsung Electronics Co., Ltd.	***3. 10:10 AM - Design and Optimization of High-Speed Packages for the Chiplet Era*** Meenakshi Upadhyaya, Srikrishna Sitaraman, Chander Ravva, Arshiya Vohra, Roxana Vladuta, Luciana Chitu, Ting Zheng – Marvell Technology, Inc.	***3. 10:10 AM - Peridynamics Enabled Digital Image Correlation for Small Scale Defect Detection*** Erdogan Madenci – University of Arizona; Amin Yaghoobi – Global Engineering Research and Technologies; Mostafa Hassani – Cornell University
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Board-Level Assembly Challenges and TIM Selections for the Large-Size FCBGA Packages Chengjian Wang, Yangfan Zhong, Xianfeng Chen, Yangyang Xu – Alibaba Group; Wenchao Wang – Jiashan Fudan Research Institute; Chuan Chen – Chinese Academy of Science-Institute of Microelectronics	***4. 11:15 AM - Power Integrity and Circuit Characteristics of Integrated Voltage Regulator (IVR) in CoWoS® Advanced Packaging Technology*** Chuei-Tang Wang, Yen-Ming Chen, Yuhuan Chen, Shu-An Shang, Yu-Ming Hsiao, Kai-Yi Tang, Kuo-Ching Hsu, Ching-Hui Chen, Mirng-Ji Lii, Kam Heng Lee, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 11:15 AM - DiffChip: Fast Chiplets Design by Automatic Differentiation*** Giuseppe Romano – Massachusetts Institute of Technology; Nima Dehmam, Xin Zhang, Arvind Kumar, Cheng Chi – IBM Corporation; Aakrati Jain – IBM Research
5. 11:35 AM - Yield Prediction Technology: A Game Changer for Cutting Costs and Reducing Ramp Time in FOPLP Lithography John Chang, Keith Best, Jian Lu, Timothy Chang – Onto Innovation	***5. 11:35 AM - Multi-Chiplet Power Delivery Network Co-Optimization Considering Current Spectrum by Deep Reinforcement Learning-Based Decoupling Capacitor Placement*** Haeseok Suh, Hyunjun An, Haeyeon Kim, Keeyoung Son, Joungho Kim – Korea Advanced Institute of Science and Technology	***5. 11:35 AM - Support Vector Algorithm-Driven Simulation for Predicting Mechanical Performance in High-Power Modules*** Chang-Chun Lee, Jui-Chang Chuang, Wei-Cheng Tsai, Yan-Yu Liou – National Tsing Hua University
6. 11:55 AM - Glass-Core Advanced Packaging Substrate Post-Dicing Die Strengths Comprehensive Comparisons for Different Singulation Methods - Dicing Induced SeWaRe Failures Re-Visited Ten Years Later Frank Wei, Andrew Frederick – DISCO Corporation	***6. 11:55 AM - RF Si Interposer Platform for Advanced Chiplet-Based Heterogeneous Systems*** Xiao Sun, Siddhartha Sinha, Hamideh Jafarpoorchekab, Melina Lofrano, Vladimir Cherman, Damien Leech, Angel Uruena – imec; Martijn Huynen – Ghent University	***6. 11:55 AM - Advanced Numerical Modeling of Microstructure Effect on Fine Cu Redistribution Lines Under Electric Current Stressing*** Tai-Yu Pan, Wen-Dung Hsu – National Cheng Kung University; Min-Yan Tsai, Yung-Sheng Lin, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)
7. 12:15 PM - Fundamental Transmission Performance Evaluation of Sub-2 Micron Fine-Wiring on Glass Core Substrate Masaya Tanaka, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.	***7. 12:15 PM - A Heterogeneous Integrated Low Noise Amplifier With High-Q Si-Interposer Inductor for Dual (Ka/V)-Band Millimeter Wave Applications*** Mei Sun, Dan Lei Yan, Jun Wei Ong, Pei Siang Lim, Binte Kuyob Nur, Jia Qi Wu, Yong Liang Ye, Teck Guan Lim – Institute of Microelectronics A*STAR	***7. 12:15 PM - Deep Clustering Based Boundary-Decoder Net for Inter and Intra Layer Stress Prediction of Heterogeneous Integrated IC Chip*** Kart Leong Lim, Ji Lin – Institute of Microelectronics A*STAR

Program Sessions: Wednesday, May 28, 2:00 p.m. - 5:05 p.m.

Session 7: High Performance Computing and Design Challenges and Solutions	Session 8: Novel Structures and Processes for Chip-to-Wafer Hybrid Bonding	Session 9: Co-Packaged Optics and Hybrid Bonding Innovations for HI
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Monita Pau** **Onto Innovation** **Email: monita.pau@ontoinnovation.com** **Eric Tremble** **Marvell Technology, Inc.** **Email: etremble@marvell.com**	**Session Co-Chairs** **Katsuyuki Sakuma** **IBM Research** **Email: ksakuma@us.ibm.com** **Dingyou Zhang** **Broadcom, Inc.** **Email: dingyouzhang.brcm@gmail.com**	**Session Co-Chairs** **Jae Kyu Cho** **GlobalFoundries, Inc.** **Email: jaekyu.cho@globalfoundries.com** **Mark Poliks** **Binghamton University** **Email: mpoliks@binghamton.edu**
1. 2:00 PM - Fine Pitch High Density CoWoS-R Package With 1.4/1.4 µm RDL Lines and 3 µm via CD Kathy Yan, Yu-Hsiang Hu, Chien-Hsun Lee, Hsin-Yu Chen, Monsen Liu, Eric Chen, Ming-Chih Yew, Chia-Kuei Hsu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 2:00 PM - 2 µm Pitch Direct Die-to-Wafer Hybrid Bonding Using Surface Protection During Wafer Thinning and Die Singulation*** Ye Lin, Pieter Bex, Samuel Suhard, Boyao Zhang, Fulya Ulu Okudur, Amaia Diaz De Zerio, Naveen Reddy, Efrain Altamirano Sanchez – imec	***1. 2:00 PM - Demonstration of Co-Packaged Optics Assembly for Fiber-Based Optical Interconnect*** Vidya Jayaram, Michael Baker, Jesus Nieto Pescador, Edidiong Udofia, Albert Lopez, Gustavo Beltran, Wei Gong, Abid Ameen – Intel Corporation
2. 2:20 PM - Development of Embedded Multi Si Bridge Package in Panel Level Process for HPC/AI Applications Hyeji Han, Jieun Park, Mijin Park, Jeongho Lee, Wonkyung Choi, Daewoo Kim – Samsung Electronics Co., Ltd.	***2. 2:20 PM - Innovative Cool-Stacking Technology for High Performance and Energy-Efficiency SoIC®*** Terry Ku, C.H. Tsai, Cheng-Chieh Hsieh, J.C. Twu, R.F. Tsui, S.W. Lu, C.S. Liu, Douglas C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***2. 2:20 PM - Optical Multi-Die Interconnect Bridge (OMIB) Interposer Assembly Process to Enable High-density Photonic Interconnects for HPC Applications*** Ankur Aggarwal – Celestial AI
3. 2:40 PM - Self-Alignment of Active Si Bridge Using Solder Joint Capillary Forces Thomas Lesueur, David Danovitch, Dominique Drouin – University of Sherbrooke; Sayuri Kohara, Akihiro Horibe – IBM Research, Tokyo; Divya Taneja, Isabel De Sousa – IBM Canada, Ltd.	***3. 2:40 PM - Influences of Chip Shape on Scaling in Chip-on-Wafer Hybrid Bonding*** Koki Onishi, Sotetsu Saito, Toru Osako, Takaaki Hirano, Naoki Ogawa, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***3. 2:40 PM - Advanced Glass Substrate Fabrication and Metallization Process Technology for Co-Packaged Optics*** Seong-Ho Seok, Bo-Kyung Kong, Kyeong-Gon Choi, Han-Yeom Lee, Jung-Hyun Noh – Corning Technology Center Korea; Lars Brusberg – Corning, Inc.
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - BBCube 3D: Fully Vertical Heterogeneous Integration of DRAMs and xPUs Using a New Power Distribution Highway Norio Chujo, Hiroyuki Ryoson, Koji Sakui, Shinji Sugatani, Masao Taguchi, Takayuki Ohba – Institute of Science Tokyo	***4. 3:45 PM - Direct Transfer Bonding Technology Enabling 50-nm Scale Accuracy for Die-to-Wafer 3D/Heterogeneous Integration*** Ichiro Sano – TAZMO Co., Ltd.; Masanori Yamagishi, Shinya Takyu, Tomoka Kirihata – LINTEC Corporation; Ryoya Kitazawa – ULVAC, Inc.; Takafumi Fukushima – Tohoku University; Yoichiro Kurita – Tokyo Institute of Technology	***4. 3:45 PM - Self-Formed Barrier Using Cu-Mn Alloy Seed Applied to a 400nm Pitch Wafer-to-Wafer Hybrid Bonding Technology*** Stefaan Van Huylenbroeck, Soon Aik Chew, Boyao Zhang, Emmanuel Chery, Joke de Messemaeker, Prafulla Gupta, Nicolas Jourdan, Sven Dewilde – imec
5. 4:05 PM - EMIB-TSV Advanced Packaging Technology - EMIB™s Next Evolution Gang Duan – Intel Corporation	***5. 4:05 PM - Hierarchical Multi-layer and Stacking Vias With Novel Structure by Transferable Cu/Polymer Hybrid Bonding for High Speed Digital Applications*** Lee Ou-Hsiang Chia-Hsin Lee, Hsiang-Hung Chang, Wei-Lan Chiu, Shih-cheng Yu, Wei-Chung Lo, Chin-Hung Wang – Industrial Technology Research Institute; Alvin Lee, Chung-An Tan – Brewer Science, Inc.	***5. 4:05 PM - SiCN CMP Integration for Hybrid Bonding Application*** Prayudi Lianto, Rachel Emmanuelle Raphael, Avery Tan, Ching Keat Chia, Xiaobo Li, Hui Min Lee, Xiaodong Chen – Applied Materials, Inc.
6. 4:25 PM - Co-Packaged Optics (CPO) Technology Full Module Test Vehicle Demonstrations John Knickerbocker, Jean Benoit Heroux, Adrian Paz Ramos, Hsianghan Hsu, Neng Liu, Yoichi Taira, Daniel Kuchta, Mark Schultz – IBM Corporation	***6. 4:25 PM - Scalable Chip-to-Wafer Hybrid Bonding Processes for Fine-pitch (3 µm and 6 µm) Interconnections*** Chandra Rao B. S. S., Arvind Sundaram, Mishra Dileep, Yong Liang Ye, Ratan Bhimrao Umralkar, Vasarla Nagendra Sekhar – Institute of Microelectronics A*STAR; Patrick Lim, Santosh Kumar Rath – Applied Materials, Inc.	***6. 4:25 PM - Inter-Die Hybrid Cu/Diamond Microbump Bonding for 3D Heterogeneous Integration*** Zhengwei Chen, Keyu Wang, Noah Opendo, Tiwei Wei – Purdue University; Shusmitha Kyatam, Joana Catarina Mendes – University of Aveiro
7. 4:45 PM - Signal, Power, and Thermal Integrity Co-Design for AI Accelerator ASIC and HBM3 on Silicon Interposer 2.5D-IC Chiplet Integration Ming-Hung Wu, Chun-Hong Chen, Chi-Lou Yeh, Chi-Ming Yang, Eric Lin, Sheng-Fan Yang – Global Unichip Corporation	***7. 4:45 PM - Advanced Metrology for Heterogeneous Chiplet Integration With 100% (Chip-to-Wafer Hybrid Bond) Overlay Control at High Speed With Four Parameter Modeling*** Bhaskar Jyoti Krishnatreya, Tan Nguyen, Siyan Dong – Intel Corporation; Frank Boegelsack, Elisabeth Brandl, Thomas Uhrmann – EV Group	***7. 4:45 PM - First Demonstration of Superior Characteristics of Co-Co Bonding With Passivation Structure at Low Thermal Budget for Advanced Packaging and Ultra-Fine Pitch Applications*** Li-Hsin Cheng, Chiao-Yen Wang, Kai-Fang Lai, Mu-Ping Hsu,, Kuan-Neng Chen – National Yang Ming Chiao Tung University

Program Sessions: Wednesday, May 28, 2:00 p.m. - 5:05 p.m.

Session 10: High Reliability Applications	Session 11: Emerging Trends: Towards High Speed, Secure, Reliable, and Sustainable Packaging	Session 12: Advanced Thermal Management Modeling
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Nokibul Islam** **STATS ChipPAC, Ltd.** **Email: nokibul.islam@statschippac.com** **Paul Tiner** **Texas Instruments, Inc.** **Email: p-tiner@ti.com**	**Session Co-Chairs** **Maria Gorchichko** **Applied Materials, Inc.** **Email: maria_gorchichko@amat.com** **Hongqing Zhang** **IBM Corporation** **Email: zhangh@us.ibm.com**	**Session Co-Chairs** **Kuo-Ning Chiang** **National Tsing Hua University** **Email: knchiang@pme.nthu.edu.tw** **Xuejun Fan** **Lamar University** **Email: xuejun.fan@lamar.edu**
1. 2:00 PM - Automotive Application-Driven Vibration Test Approach: Bridging the Gap Between Module and Board Level Reliability Test Methods Varun Thukral, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc; C. Chou – NXP Semiconductors, Inc/Delft University of Technology; Ovidiu Vermesan – SINTEF Digital; Willem Driel – Delft University of Technology	***1. 2:00 PM - Lumped Element Multiplexer Design and Calibration in Cryogenic Environment for Quantum Reflectometry Applications*** Vignesh Shanmugam Bhaskar, Mihai Rotaru – Institute of Microelectronics A*STAR	***1. 2:00 PM - Development of an Embedded 2-Phase Cooling Technology for Two Stacked High-Power Chips in Future HPC & AI Applications*** Xiaowu Zhang, Huicheng Feng, Gongyue Tang, Boon Long Lau, Jun Wei Javier Ong, Ming Chinq Jong, Surya Bhattacharya, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR
2. 2:20 PM - Chip Package Interaction Challenges and Solutions for FOWLP Product Reliability for Automotive Applications Gaurav Sharma, Amar Mavinkurve, Michiel Soestbergen, Greta Terzariol, Taki Fang, Nishant Lakhera – NXP Semiconductor, Inc.	***2. 2:20 PM - Embedded Silicon Chip Capacitors in Glass Package for Vertical Power Delivery*** Ramin Rahimzadeh Khorasani, Mohammad Al-Juwhari, Madhavan Swaminathan – Pennsylvania State University; Xingchen Li – Georgia Institute of Technology	***2. 2:20 PM - Graphite Sheet Embedded in an Organic Flip-Chip Package for Heat Spreading*** Keiji Matsumoto, Daisuke Oshima, Hiroyuki Mori, Toyohiro Aoki, Akihiro Horibe – IBM Research, Tokyo; Atom Watanabe, Russell Budd – IBM Research; Daniel Edelstein – IBM Corporation
3. 2:40 PM - Higher Reliability Cu Pillar Bump on ENEPIG Substrate With Suppressed Ni3P for Automotive Applications Hideaki Tsuchiya, Teruhiro Kuwajima, Yoshiaki Yamada, Nobuhiro Kinoshita, Koichi Ando – Renesas Electronics Corporation	***3. 2:40 PM - SiPMeter: Active Hardware Metering for Heterogeneously Integrated System-in-Packages (SiPs)*** Md Latifur Rahman, Amit Mazumder Shuvo, Jingbo Zhou, Mark Tehranipoor, Farimah Farahmandi – University of Florida	***3. 2:40 PM - Enhanced Thermal Management of a 1.2 kV SiC MOSFET Half-Bridge Fan-Out Panel-Level Packaging With Nanocopper Sintering Die-Attachment*** Wei Chen, Junwei Chen, Chao Gu, Tiancheng Tian, Jiajie Fan – Fudan University; Xuejun Fan – Lamar University; G. Q. (Kouchi) Zhang – Delft University of Technology
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Reliability and Microstructure Characterization of Through-Silicon Vias (TSV) at Different Aspect Ratios Using EBSD-Raman Spectroscopy Shuhang Lyu, Thomas Beechem, Tiwei Wei – Purdue University	***4. 3:45 PM - Advanced Metrology Suite for Linking Residual Stress to Fundamental Properties of Thermoset Packaging Materials*** Polette Centellas, Stian Romberg, Ran Tao, Gery Stafford, Alexander Landauer, Christopher Soles – National Institute of Standards and Technology	***4. 3:45 PM - Integrated Package-to-System Thermal Solution Evolution for High-Performance 2.5D CoWoS-R Advanced Packaging Technology Development*** Tsunyen Wu, Kuo-Chin Chang, Chien-Chang Wang, Bang-Li Wu, Ching Wang, Kathy Yan, Chien-Hsun Lee, Cheng-Chi Hsieh – Taiwan Semiconductor Manufacturing Company, Ltd.
5. 4:05 PM - Cryogenic and Wide Temperature Thermal Cycling Reliability Study of QFN and CQFJ Packages for Lunar Missions Harshil Goyal, Wayne Johnson, Michael Hamilton – Auburn University; Bhargav Yelamanchili – ANSYS, Inc.	***5. 4:05 PM - Predictive Modeling of IMC Growth in BGA Component Solder Joints Using Artificial Neural Networks Under Rework and Temperature Cycling Conditions*** Adlil Aizat Ismail, Muhammad Nizam Ilias – National University of Malaysia/Western Digital; Maria Abu Bakar, Azman Jalar, Mohd Ridzwan Yaakub, Muhammad Iqbal Abu Latiffi – National University of Malaysia; Erwan Basiron – Western Digital Corporation	***5. 4:05 PM - Microfluidic Cooling of Heterogeneously Integrated HBM-GPU Module With Step Height Difference*** Euichul Chung, Muhannad Bakir – Georgia Institute of Technology
6. 4:25 PM - Thermal Aging-Induced Crack Formation in Glass Fiber Reinforced Printed Circuit Boards: The Role of Polymer Shrinkage and Oxidation Mandy Marleen Krott, Dr.-Ing. Thomas Ewald – Robert Bosch GmbH; Prof. Dr.-Ing. Holger Ruckdaeschel – University of Bayreuth	***6. 4:25 PM - Parameter Degradation Monitoring and Controller Adaptation Using Digital Twin*** Lidya Mussie Weldehawaryat, Shuofeng Zhao – National Renewable Energy Laboratory; Wajiha Shireen – University of Houston	***6. 4:25 PM - Real-Time and Scalable Thermal Management Strategy for Power-Sensitive Applications With AI-Enabled Global Optimization*** Zhi Yang, Yong Pei – Groq; Anni Zheng – Visualization Solution
7. 4:45 PM - Weibull-Norris-Landzberg Acceleration Factor Model for Indium Thermal Interface Material Wear-Out Failure Mode Amirfarzad Behnam, Kaushik Mysore – Advanced Micro Devices, Inc.	***7. 4:45 PM - Bio-Sourced Unfilled Epoxy for Die-Attach Applications*** Saria Berger, Frederic A. Banville, David Danovitch – University of Sherbrooke; Catherine Marsan-Loyer – Centre de Collaboration MiQroInnovation (C2MI); David Gendron – Kemitek; Serge Ecoffey – Universite de Sherbrooke	***7. 4:45 PM - First Demonstration of Metal-Lidded Integral Microjet Impingement On-Chip Cooling Structures With Alternating Feeding and Draining Nozzles for High-Performance Interposer Packages*** Gopinath Sahu, Ruoyi Li, Ketan Yogi, Akshat Patel, Tiwei Wei – Purdue University

Program Sessions: Thursday, May 29, 9:30 a.m. - 12:35 p.m.

Session 13: Large Panel Fan-Out for High Density Integration	Session 14: New Materials and Processes in Wafer-to-Wafer Hybrid Bonding	Session 15: Photonics Integration and Subsystems
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Photonics**
Session Co-Chairs **Lihong Cao** **Advanced Semiconductor Engineering, Inc. (US)** **Email: lihong.cao@aseus.com** **Steffen Kroehnert** **ESPAT Consulting, Germany** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs** **Wei-Chung Lo** **Industrial Technology Research Institute** **Email: lo@itri.org.tw** **Chih-Hang Tung** **Taiwan Semiconductor Manufacturing Company, Ltd.** **Email: chtungc@tsmc.com**	**Session Co-Chairs** **Takaaki Ishigure** **Keio University** **Email: ishigure@appi.keio.ac.jp** **Richard Pitwon** **Resolute Photonics, Ltd.** **Email: richard.pitwon@resolutephotonics.com**
1. 9:30 AM - Carrier Warpage Improvement Using Non-Photosensitive Dielectric Material for High I/O Density Organic RDL Application in Future Advanced Packaging. Guillermo Fernandez Zapico, Pondchanok Chinapang, Junya Miyake, Susumu Baba – Taiwan Semiconductor Manufacturing Company, Japan; Chih-Kai Cheng, Tsung-Yu Chen, Tsung-Shu Lin, Shimpei Yamaguchi – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Integration, Materials and Equipment Innovations to Enable 100 nm Pitch W2W Bonding for Memory-to-Logic and Logic-to-Logic 3D Stacking*** Raghav Sreenivasan, Kevin Ryan, Jeremiah Hebding, Tyler Sherwood, Siddarth Krishnan, Ying Trickett, Michael Chudzik – Applied Materials, Inc.; Barbara Weis – EV Group	***1. 9:30 AM - Functional Demonstrator of a 256 Channels Beam Steering Device of a LIDAR for Autonomous Driving Including Silicon Photonics, 3D and Advanced Packaging Features : TSV and Fine Pitch Flip Chip*** Thierry Mourier, Nadia Miloud-Ali, Laura Boutafa, Selimen Benahmed, Vincent Moulin, Yacoub Sahouane – CEA-LETI
2. 9:50 AM - Next Generation Panel Level RDL Interposer Package for High Density Interconnection Da-Hee Kim, Youngchan Ko, Wooseok Park – Samsung Electronics Co., Ltd.	***2. 9:50 AM - Advanced Memory Wafer-to-Wafer Bonding With Support of Recyclable Carrier Systems*** Wei Zhou, Kyle Kirby, Mota Liou, Kunal Parekh, Vladimir Noveski, Akshay Singh – Micron Technology, Inc.	***2. 9:50 AM - An Ultra-Compact 8-Channel Linear-Drive VCSEL-Based CPO Transceiver for Networks and AI/ML Applications in a Data Center*** Wataru Yoshida, Kazuya Nagashima, Kensho Nishizaki, Sho Yoneyama, Hideyuki Nasu – Furukawa Electric Co., Ltd.
3. 10:10 AM - M-Series Fan-Out Interposer Technology (M-FIT) - Scaling up for HPC & AI Craig Bishop, Robin Davis, Liberty Perez, Ryan Sanden, Andrew Hoetker – Deca Technologies, Inc.	***3. 10:10 AM - Development of Wafer-Level Wet Atomic Layer Etching Process Platform for Cu Surface Topography Control in Hybrid Bonding Applications*** Seung Ho Hahn, Wooyoung Kim, Seongmin Son, Kyu-Ha Lee, Jung Shin Lee, Joohee Jang, Kyeongbin Lim, Bumki Moon – Samsung Electronics Co., Ltd.	***3. 10:10 AM - InP/Si Integrated Laser With High-Tolerance-Multi-Step-Long-Period Diffraction Grating*** Junichi Suzuki, Masahiro Matsuura, Masakazu Takabahashi, Yosuke Suzuki, Nobuo Ohata – Mitsubishi Electric Corporation
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Enhancement of the Adhesion in Multilayered Redistribution Layers of Fan-Out Wafer Level Packages for Memory Application Kyoungtae Eun, Ki-Jun Sung, Jae-Min Kim, Se-Hyun Jang, Seowon Lee, Sungwon Yoon, Won Hae Kim, Seungchul Han – SK hynix Inc.	***4. 11:15 AM - Development of a Novel WoWoW Process for 1/1.3-inch 50 Megapixel Three-Wafer-Stacked CMOS Image Sensor With DNN Circuits*** Kan Shimizu, Ryoichi Nakamura, Wataru Otsuka, Hayato Iwamoto – Sony Semiconductor Solutions Corporation; Takumi Kamibayashi, Nobutatsu Araki, Kenichi Saitou – Sony Semiconductor Solutions; Yoshihisa Kagawa – Sony	***4. 11:15 AM - Development of Transfer-Printed III-V C-band Lasers on Silicon Photonic Integrated Circuits for Multi-Project Wafer Offering*** George Nelson, Colin McDonough, Christopher Striemer, David Harame – AIM Photonics; James O'Callaghan, Padraic Morrissey, Peter O'Brien – Tyndall National Institute; Stefan Preble – Rochester Institute of Technology
5. 11:35 AM - Die-to-Die Parallel Interface Optimization Utilizing Deca™s Novel M-Series Gen-2 Fan-Out Technology Ting Zheng, Joshua Dillon, Eric Tremble – Marvell Technology, Inc.; Craig Bishop – Deca Technologies, Inc.; Wolfgang Sauter – Marvell Semiconductor, Inc.	***5. 11:35 AM - Wafer-to-Wafer Hybrid Bonding Technology With 300nm Interconnect Pitch*** Stefaan Van Huylenbroeck, Soon Aik Chew, Boyao Zhang, Lieve Bogaerts, Cindy Heyvaert, Sven Dewilde, Serena Iacovo, Michele Stucchi – imec	***5. 11:35 AM - Laser Assisted Transfer (LAT) of Coupon of III-V Epitaxial Layer on Silicon Photonics devices*** Takenori Fujiwara, Jumpei Jumpei Oniki, Yukari Jo, Daichi Miyazaki – Toray Industries, Inc.
6. 11:55 AM - Low Loss, High Reliability (LLHR) Package on a 650 mm x 650 mm Hybrid Panel-Level Package Platform Eoin O'Toole, Jose Silva, Paulo Cardoso, Filipe Cardoso, Maria Bras, Jose Miguel Silva, Pedro Fernandes, Pedro Ferreira – Amkor Technology Portugal	***6. 11:55 AM - Electrical Performance of Hybrid Bonding With Sub-Micron Cu-Cu Bonding Contacts: Effects of Scaling, Microstructure, and Surface Morphology*** Sari Al Zerey, Alina Bennett-Dubin, Morlidhar Patel, Junghyun Cho – State University of New York at Binghamton; Roy Yu, Nicholas Polomoff, Luke Darling, Katsuyuki Sakuma – IBM Research	***6. 11:55 AM - Stress, Thermal and Optical Performance (STOP) Analysis of Co-Packaged Optical Processor With FPGA-Memory-Optics-Power Integration*** Venkata Ramana Pamidighantam, Jugal Kishore Bhandari, Ubed Mohammad, Mayuri Adepu, Vamsi Rekapally, Tanisha Jain, Raghuveer M C – LightSpeed Photonics Pte Ltd; Mihai Rotaru – Institute of Microelectronics A*STAR
7. 12:15 PM - Evolution of Advanced Packaging From FOWLP to FOPLP: Development of Fanout Chip Last With Embedded Bridge in 300 mm Panel Smith Chen, Yung Shun Chang – Advanced Semiconductor Engineering, Inc. (US)	***7. 12:15 PM - Selective Ru Deposition on Cu Bond Pads to Enable Low Thermal Budget Hybrid Bonding for HBM Applications.*** Hemanth Kumar Cheemalamarri, Nithin Poonkottil, Masahisa Fujino, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR	***7. 12:15 PM - Direct Flip Chip-on-Board Assembly (FCOB) for Optical Transceivers*** Hiren Thacker, Tong Wang – Cisco Systems, Inc.

Program Sessions: Thursday, May 29, 9:30 a.m. - 12:35 p.m.

Session 16: Manufacturing and Thermal Management Reliability	Session 17: Signal Integrity / Power Integrity for Advanced Packaging Technologies	Session 18: Simulations and Validation on Reliability Challenges of High Performance Packages
Committees: Applied Reliability and Assembly & Manufacturing Technology	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Varughese Mathew** **NXP Semiconductor, Inc.** **Email: varughese.mathew@nxp.com** **Venkata Mokkapati** **AT&S AG** **Email: v.mokkapati@ats.net**	**Session Co-Chairs** **Amit P. Agrawal** **Advanced Micro Devices, Inc.** **Email: amit.agrawal@amd.com** **Xiao Sun** **imec** **Email: xiao.sun@imec.be**	**Session Co-Chairs** **Ruiyang Liu** **TeraDAR Inc.** **Email: ruiyang.liu9@gmail.com** **Karsten Meier** **TU Dresden** **Email: karsten.meier@tu-dresden.de**
1. 9:30 AM - Influence of Sn-Bi Solder Joints Microstructure on the Electrical and Joule Heat Properties Nathaniel Power, Choong-Un Kim, Pushkar Gothe – University of Texas, Arlington; Tae-Kyu Lee, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.	***1. 9:30 AM - Simulation and Optimization of 32Gbps On-Interposer Interconnects With Novel Deep Trench Based Equalizer*** Changming Song, Xiuyu Shi, Qian Wang, Jian Cai – Tsinghua University; Shengjuan Zhou – Tsinghua University, Shanghai	***1. 9:30 AM - Simulation and Experimental Validation of Microstructure Evolution of Sintered Ag Layer During Thermal Aging Using a Hybrid Potts-Phase Field Model*** Xiao Hu, Qilin Xing, Marcel Hermans, Willem van Driel – Delft University of Technology; Jianlin Huang, Hans van Rijckevorsel, Huib Scholten – Ampleon B.V.; Rene Poelma – Nexperia
2. 9:50 AM - A Study on the Improvement of Solder Joint Reliability of Module Products by IPL Soldering Method Myeong-Hyeon Yu, Jaeseon Hwang, Taegyu Kang, Jongho Lee – Samsung Electronics Co., Ltd.	***2. 9:50 AM - Mixed-Mode Distributed Physical-Based Transmission Line Model for Fast Signal Integrity Analysis on the S-Parameter Resonances and PAM4 Transmission of 5G Connectors*** Yulin He, Kewei Song, Haonan Wu, Milton Feng – University of Illinois	***2. 9:50 AM - Enabling Comprehensive Study of Electromigration and Diffusion Induced Failure Mechanisms in Lead-Free Solder Joint by Frame of Phase Field Modeling*** Harikrishnan Kumarasamy, Choong-Un Kim – University of Texas, Arlington; Hariram Mohanram – United Test and Assembly Center, Ltd.; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.
3. 10:10 AM - Improving the Quality and Yield Performance of Vacuum Fluxless Reflow Soldering for High-Density AI Chips Lei Jing, Xinxuan Tan, Anderson Chen, Vladimir Kudriavtsev, Wayne Chen, Hans Lin, Zia Karim, Saket Chadda – Yield Engineering Systems	***3. 10:10 AM - Signal Integrity Analysis of Differential Through-Silicon Via (TSV) With Silicon Dioxide Well (SDW) for Impedance Compensation in the Serdes Interface*** Hyunwoong Kim, Sungwook Moon, Jiyoung Park, Seungki Nam – Samsung Electronics Co., Ltd.	***3. 10:10 AM - In-Situ Confocal Raman Spectroscopy Assisted Interfacial Residual Stress Characterization in SiC Chip Sintered on AMB Substrate With Nanocopper Paste*** Xuyang Yan, Zhoudong Yang, Chao Gu, Tiancheng Tian, Jiajie Fan – Fudan University; Xuejun Fan – Lamar University; G. Q. (Kouchi) Zhang – Delft University of Technology
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Additive Low-Temperature Assembly on Sustainable Substrates Circuit Reliability Performance and Stability Interactions Pradeep Lall, Daniel Karakitie, Shriram Kulkarni, Md Golam Sarwar – Auburn University; Scott Miller – NextFlex	***4. 11:15 AM - Software-Defined Power Integrity (PI) Analysis for 2.5D/3D Packages*** Wei Zhang, Chander Rawa, Moutasem Eltawil, Meenakshi Upadhyaya, Srikrishna Sitaraman, Arshiya Vohra, Ellie Baghernia, Narayan Agnihotri – Marvell Technology, Inc.	***4. 11:15 AM - Additively Manufactured In-Mold Electronics Reliability Under Thermal Cycling and Sustained High Temperature*** Pradeep Lall, Fatahi Musa, Shriram Kulkarni, Md Golam Sarwar – Auburn University; Scott Miller – NextFlex
5. 11:35 AM - Investigation on Joule Heating of Plated Through Hole (PTH) Via Howard Gan, Antai Xu, Jeffrey Zhang – Advanced Micro Devices, Inc.	***5. 11:35 AM - Power Integrity Design of a 56Gb/s Si-Photonic Optical Link for Memory Applications*** Sagar Dubey, Dan Oh, Sam Khalili, Suresh Pothukuchi, Ankur Aggarwal – Celestial AI	***5. 11:35 AM - Thermal-Mechanical Modeling of Package Reflow for Cooling of Future CPU and GPU Devices*** Ercan (Eric) Dede, Shailesh Joshi – Toyota Research Institute North America; Paul Paret, Gilbert Moreno, Sreekant Narumanchi – National Renewable Energy Laboratory; Suhas Tamvada, Saeed Moghaddam – University of Florida; Patrick McCluskey – University of Maryland
6. 11:55 AM - Thermo-Mechanical Stability of High-Performance Chip Integration: Structure-Induced Stress in Complex System Structures Yujin Park, Tae-Kyu Lee, Yawei Li, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.	***6. 11:55 AM - Signal Integrity Design of a High-Performance, High-Frequency (10MHz to 11GHz), 3dB Bandwidth High-Speed ADC Driver Amplifier*** Rajen Murugan, Li Jiang – Texas Instruments, Inc.; Tony Tang – IEEE	***6. 11:55 AM - Development and Optimization of a Flexible Printed Coplanar Capacitive Sensor for Accurate Twisting Motion Detection*** Colleen Stover, Rui Chen, Yuxuan Hou – Eastern Michigan University
7. 12:15 PM - Enhanced Electromigration Reliability of Cu/SiO2 Hybrid Joints Fabricated by (111)-Oriented Nanotwinned Cu Shih-Chi Yang – National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang – Industrial Technology Research Institute; Chih Chen – National Yang Ming Chiao Tung University	***7. 12:15 PM - Compact Tri-Band Stub Filter Using Advanced Bridged-CRLH Transmission Line for 5G Applications*** Junhyuk Yang, Hanna Jang, Yong-Kyu Yoon – University of Florida	***7. 12:15 PM - Isothermal Shock Testing and Failure State Analysis on Flip-Chip Interconnects*** Max Frank Haeusler, Karsten Meier, Shengxiang Lyu, Karlheinz Bock – TU Dresden

Program Sessions: Thursday, May 29, 2:00 p.m. - 5:05 p.m.

Session 19: Chiplet Integration and Advanced Thermal Solutions	Session 20: Novel Technologies for High Density RDL Interposers	Session 21: Meeting AI Challenges : Large Package Solution and Warpage Management for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Young-Gon Kim** **Renesas Electronics Corporation** **Email: young.kim.jg@renesas.com** **Luu Nguyen** **PsiQuantum** **Email: lnguyen@psiquantum.com**	**Session Co-Chairs** **Nathan Lower** **Consultant** **Email: nplower@hotmail.com** **Tiwei Wei** **Purdue University** **Email: wei427@purdue.edu**	**Session Co-Chairs** **Bing Dang** **IBM Corporation** **Email: dangbing@us.ibm.com** **Frank Wei** **DISCO Corporation** **Email: frank_w@discousa.com**
1. 2:00 PM - Direct-to-Silicon Liquid Cooling Integrated on 3.3x CoWoS-R Platform Yu-Jen Lien, Sing-Da Jiang, Han-Jong Chia, Tsunyen Wu, Cheng-Chieh Hsieh, Kuo-Chung Yee, Kathy Yan, Douglas C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 2:00 PM - Pillar-Suspended Bridge (PSB); Transmission Simulation and Fabrication Process of 2-Micron Diameter / 5-Micron Pitch Dry Etched Stacked Via in Low-k Polymer for High Performance RDL Bridge*** Shinichi Arioka, Tanapun Srichanthamit – AOI Electronics; Yusuke Naka, Koh Meiten – Taiyo Ink Mfg. Co., Ltd.; Fumito Otake, Yasuhiro Morikawa – ULVAC, Inc.; Osamu Okada – Institute of Science Tokyo; Yoichiro Kurita – Tokyo Institute of Technology	***1. 2:00 PM - Containment Solution for Liquid Metal-Based Second-Level Interconnect Technology*** Ziyin Lin, Karumbu Meyyappan, Taylor Rawlings, Dingying Xu – Intel Corporation
2. 2:20 PM - A Novel Approach of Multi-Chip FOPKG Chiplet Interconnection Using a Land-Side Si Bridge Sungoh Ahn, Eunkyeong Park, Seokbeom Yong, Junghoo Yun, Dongsuk Kim, Heeyoub Kang, Sangkyu Lee, Jongyoun Kim – Samsung Electronics Co., Ltd.	***2. 2:20 PM - Panel Level Interposer by Using Glass Carrier for 2.5D Advance IC Package Application*** Terry Wang, Cheng-Yueh Chang, William Yang, Yu-Jhen Yang, Pei-Pei Cheng, Chien-Ming Tseng – Industrial Technology Research Institute; Hungyu Wu – Applied Materials, Inc.; Austin Cheng – FAVITE, Inc.	***2. 2:20 PM - Ultra High Aspect Ratio Photo Resist for Cu Pillar Based Multi-Stack Fan-out Package With Wide I/O LPDDR*** Seon Ho Lee, Jinyoung Kim, Jeongseok Mun, JunHyeong Park, Jihye Shim, YoungGwan Ko – Samsung Electronics Co., Ltd.
3. 2:40 PM - Mid-BEOL Heterogeneous Integration Through Sub-1 µm Pitch Hybrid Bonding & Advanced Silicon Carrier Technologies for AI & Compute Applications Adel A Elsherbini, Tushar Talukdar, Paul Nordeen, Thomas Sounart, Brandon Rawlings, Andrey Vyatskikh, Feras Eid, Saurabh Chauhan, – Intel Corporation	***3. 2:40 PM - Fine Pitch Semi-Additive RDL-Process Development*** Nelson Pinho, Lili Wang, Murat Pak, Punith Kumar Mudiger Krishne Gowda, Amaia Diaz De Zerio, Jeonho Kim, Andy Miller, Eric Beyne – imec	***3. 2:40 PM - Advanced FO PLP Digital Lithography Patterning Development for AI Devices*** Ksenija Varga, Roman Holly, Boris Povazay, Tobias Tobias, Thomas Uhrmann – EV Group; Marieke Vandevyvere, Niels Van Herck – Fujifilm Electronic Materials
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - The Study and Challenges of Backside Metal Interface Material to Enhance Fan-Out Embedded Bridge Die Package (FO-EB) Thermal Performance Kuei Hsiao Kuo, Jui Teng Hung, Ting En Lin, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.	***4. 3:45 PM - Wafer Backside Fine Pitch Copper Interconnects and Low-Profile Micro-Bumps Pad Process for Multiple Chip-on-Wafer Stacking Structure*** Syuto Tamura, Junichiro Fujimagari, Yuji Uesugi, Kenta Fukushima, Kota Maruyama, Takuji Matsumoto, Kentaro Akiyama – Sony Semiconductor Solutions	***4. 3:45 PM - Effective Build-Up Substrate Design for Warpage Reduction and Reliability Enhancement in Advanced Semiconductor Packages*** Daichi Okazaki, Eiji Baba, Yuto Inoue, Ikumi Sawa, Daisuke Hironiwa, Ryo Miyamoto – Ajinomoto Fine-Techno Co., Inc.; YoungGun Han, Taka Kanayama – Fukuoka University
5. 4:05 PM - Thermal Impact of BSPDN for 3D Memory and Logic Integration Melina Lofrano, Herman Oprins, Geert Van der Plas, Eric Beyne – imec	***5. 4:05 PM - Reliability Assessment of a Hybrid Wiring Layer Assembly for Low-Cost Sub 10 µm Pitch Integration*** Vineeth Harish, Krutikesh Sahoo, Subramanian Iyer – University of California, Los Angeles; Kai Zheng, Gilbert Park, Han-Wen Chen, Steven Verhaverbeke – Applied Materials, Inc.	***5. 4:05 PM - Development of Negative Thermal Expansion Zeolite Fillers for Next-Generation Low CTE Encapsulation Materials*** Ryo Nishida, Masahiro Yokoyama, Yutaro Tanaka, Ryoji Onishi, Syu Hikima, Kazuki Tsujikawa – Mitsubishi Chemical Corporation
6. 4:25 PM - Inter-Die Gap-Filling With Varying Aspect Ratio (AR) Using PECVD Oxide for 3D Packaging: Model Prediction and Experimental Validation Md Mahbubul Hasan, Rajesh Surapaneni, Yuting Wang, Pilin Liu, Xavier Brun – Intel Corporation	***6. 4:25 PM - A Novel Architecture for On-Device AI in Mobile Application With Enhanced Heat Dissipation*** Kyung Don Mun, Jihwang Kim, Sangjin Baek, Jaechoon Kim, Suk Won Jang, Kang Joon Lee, DongWoon Park, Daewoo Kim – Samsung Electronics Co., Ltd.	***6. 4:25 PM - Development of Novel Photosensitive Polyimide With 170 °C Curing Process to Enable Low Warpage and sub-2 µm Patterning for RDLs in Next Generation Interposer*** Yusuke Murata, Shuhei Horikawa, Mitsuka Inoue, Ryoji Tatara, Hirokazu Ito – JSR Corporation
7. 4:45 PM - Fabrication and Performance of Silicon-Based Ultra-Thin Heat Spreading Die Juno Kim, Seokjun Lee, Jung Shin Lee, Kyeongbin Lim, Hyunhee Kim, Minwoo Rhee – Samsung Electronics Co., Ltd.; Young Jong Lee, Sung Jin Kim – Korea Advanced Institute of Science and Technology	***7. 4:45 PM - High-Density RDL Fan-Out with L/S 2/2µm Dry-Etched Micro Vias for Agile Prototyping/Low-Volume Production and TAT/NRE Cost Modeling*** Yuichi Sukegawa, Kenji Miyake – Maxell, Ltd.; Osamu Okada – Institute of Science Tokyo; Takafumi Fukushima, Hiroyuki Hashimoto – Tohoku University; Yusuke Naka – Taiyo Ink Mfg. Co., Ltd.; Yasuhiro Morikawa – ULVAC, Inc.; Akira Shimada – Toray Industries, Inc.; Yoichiro Kurita – Tokyo Institute of Technology	***7. 4:45 PM - Innovative Silicon Die Thinning and Edge Protection of Chip-to-Wafer Hybrid Bonded Wafer for High-Density Multi-Chip Stacking*** Vasarla Nagendra Sekhar, Mishra Dileep, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR; Roman Ivanov – Entegris, Inc.; Subhash Guddati – Entegris Asia Pte. Ltd.

Program Sessions: Thursday, May 29, 2:00 p.m. - 5:05 p.m.

Session 22: Heterogeneous Integration Using Bridge and 3D Stacking	Session 23: AI Enabled Innovations in Advanced Packaging Technologies	Session 24: Advanced Characterization and Modeling of Next Generation Packaging Materials
Committee: Assembly & Manufacturing Technology	**Committees: Electrical Design and Analysis and Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Pascale Gagnon** **IBM Canada, Ltd.** **Email: pgagnon@ca.ibm.com** **Omkar Gupte** **Advanced Micro Devices, Inc.** **Email: Omkar.Gupte@amd.com**	**Session Co-Chairs** **Xinpei Cao** **Henkel Corporation** **Email: xinpei.cao@henkel.com** **Hideki Sasaki** **Rapidus Corporation** **Email: hideki.sasaki@rapidus.co.jp**	**Session Co-Chairs** **Rui Chen** **Eastern Michigan University** **Email: rchen7@emich.edu** **Ning Ye** **Western Digital Corporation** **Email: ning.ye@wdc.com**
1. 2:00 PM - Hybrid Bonding With Fluidic Self Alignment: Process Optimization and Electrical Test Vehicle Fabrication Feras Eid – Intel Corporation	***1. 2:00 PM - AI-Based Decision-Tree Concept to Fabricate Active Wafer Scale Fabric for Heterogeneous Chiplet Integration*** Rabindra Das, Albert Reuther, Vitaliy Gleyzer, Ryan Touzjian, Alex Wynn, Ravi Rastogi, Brian Tyrrell, Paul Monticciolo – MIT Lincoln Laboratory	***1. 2:00 PM - Characterization of Moisture Diffusion Properties of ABF and Mold Compounds in Molded Package With High Copper Density Substrate*** S M Yeasin Habib, Xuejun Fan – Lamar University; Guangxu Li, Yutaka Suzuki, Jonathan Noquil, Mak Kulkarni, Rajen Murugan – Texas Instruments, Inc.
2. 2:20 PM - Investigation of Bonding Signatures Induced by Wafer-to-Wafer (W2W) Bonding and Implementation of High Order Corrections per Exposure (HOCPE) During Backside EUV Litho Processing in CFET Technology Sujan Kumar Sarkar, Andrea Mingardi, Rajendra Kumar Saroj, Sandip Halder – imec	***2. 2:20 PM - AI Trustworthiness in the Era of Advanced Packaging: Challenges and Opportunities*** Katayoon Yahyaei, Mohammad Shafkat Khan, Anirban Bhattacharya, Baibhab Chatterjee, Navid Asadizanjani – University of Florida; Parth Sandeepbhai Shah – Intel Corporation	***2. 2:20 PM - Thermal-Mechanical Behavior of Highly (111)-Oriented Nano Twinned Electroplated Copper for Advanced Electronic Packaging*** Abdellah Salahouelhadj, Kris Vanstreels, Joke de Messemaeker, Aleksandar Radisic, Zaid El-Mekki, Carine Gerets – imec; Iris Chang – BASF Taiwan; Sung-Ho Park – BASF Korea
3. 2:40 PM - Assessing Queue Time in D2W Hybrid Bonding Through Precise Bond Strength Measurements Yuki Yoshihara, Junya Fuse, Fumihiro Inoue – Yokohama National University; Shimpei Aoki, Takashi Hare, Kentaro Mihara, Takayuki Miyoshi – Toray Engineering Co., Ltd.; Naoko Yamamoto, Shunsuke Teranishi – DISCO Corporation; Atsushi Oda – Disco Corporation; Takafumi Fukushima – Tohoku University; Akira Uedono – University of Tsukuba	***3. 2:40 PM - Efficient Visual Inspection Framework of High-Bandwidth Memory Bumps With Generative and Deep Learning AI*** Richard Chang, Ramanpreet Singh Pahwa, Jie Wang, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong – Institute of Microelectronics A*STAR	***3. 2:40 PM - Revealing Oxidation-Induced Mechanical Degradation in Nano-Cu Sintering via Micro-Cantilever Bending Tests*** Weiping Jiao, Leiming Du, G. Q. (Kouchi) Zhang – Delft University of Technology; Olof Baecke, Magnus Hörnqvist Colliander – Chalmers University of Technology; Emiel de Bruin, Lingen Wang – Boschman Advanced Packaging Technology B.V.
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Thin 3D: an Innovative Approach to Ultra-Thin Wafer-Level Active Device Transfer Technology With Optimized Material and Thermal Solution for 3D IC Ting-Yu Chen, Shie-Ping Chang, Bo-Jheng Shih, Zih-Yang Chen, Yu-Lun Liu – National Yang Ming Chiao Tung University; Po-Jung Sung, Nien-Chih Lin, Chih-Chao Yang – Taiwan Semiconductor Research Institute	***4. 3:45 PM - Generative Model Based Multi-Layer PDN Impedance Estimation With Multi-Power Domain*** Hyunjun An, Haeseok Suh, Keeyoung Son, Haeyeon Kim, Joungho Kim – Korea Advanced Institute of Science and Technology	***4. 3:45 PM - Non-PFAS Semiconductor Packaging Material Performance and Stability in Comparison With PFAS Materials*** Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Madhu Kasturi – Auburn University
5. 4:05 PM - Ultra-Thin Wafer Handling Process for Advanced Packaging Using Novel Temporary Bonding Film and De-Bonding Method Motohiro Negishi, Yuta Akasu, Emi Miyazawa, Tetsuya Enomoto, Kohei Taniguchi, Takashi Kawamori – Resonac Corporation; Hochoong Lee – Teikoku Taping System Co., Ltd.	***5. 4:05 PM - RAICEx: a Rapid and Accurate AI-Based Framework for Crosstalk Prediction in IC Packages With a Case Study on High-Speed DDR Systems*** Katayoon Yahyaei, Tapobrata Bandyopadhyay, Snehamay Sinha – Texas Instruments, Inc.	***5. 4:05 PM - Predictive Modeling of Thin Films Properties Using an Experimental and Simulation-Based Approach*** Dao Kun Lim – National University of Singapore/Micron Technology; Derik Rudd, Venkata Rama Satya Pradeep Vempaty, Wen How Sim, Harjashan Veer Singh – Micron Technology, Inc.; Faxing Che – Micron Semiconductor Asia Operations Pte. Ltd; Wentao Yan, Yeow Kheng Lim – National University of Singapore
6. 4:25 PM - A Novel Thermal Isolation Method With Embedded Glass Bridge™ Structures in Silicon-Based 3D Heterogeneous Integration Systems Zhengwei Chen, Feifan Xie, Tiwei Wei – Purdue University	***6. 4:25 PM - TDR Optimization Method of 112G Serdes Interface in PKG Using Deep Reinforcement Learning*** Hyunwoong Kim, Sungwook Moon, Jiyoung Park, Taeyun Kim, Jinho Kim, Haemin Lee, Seungki Nam – Samsung Electronics Co., Ltd.	***6. 4:25 PM - Physics-Based Modeling With Nanoindentation on the Mechanical Reliability of TGV Substrates Under Annealing Effects*** Jui-Chang Chuang, Wei-Cheng Tsai, Hao-Zhou Lin, Chen-Tsai Yang, Chung-I Li – Industrial Technology Research Institute; Chang-Chun Lee – National Tsing Hua University; Shih-Hsien Lee, Shih-Hao Kuo – Applied Materials, Inc.
7. 4:45 PM - FOCoS-Bridge for Emerging Trends in High-Performance Computing (HPC) and Artificial Intelligence (AI) Smith Chen – Advanced Semiconductor Engineering, Inc. (US)	***7. 4:45 PM - AI-Assisted Electro-Thermal Co-Design for Hybrid Bonded Packages*** Juhitha Konduru, Jose Schutt-Aine – University of Illinois; Srikanth Rangarajan – Binghamton University	***7. 4:45 PM - Validated Methodology for Accurate Simultaneous Measurement of Elastic Modulus and CTE of BEOL Materials for Improved Advanced Package Performance Prediction*** Chukwudi Okoro – Corning Research and Development Corp.; James Price, Diego Prado, Alex Longacre, Nicholas Walker, Shandon Hart – Corning, Inc.

Program Sessions: Friday, May 30, 9:30 a.m. - 12:35 p.m.

Session 25: Advanced Substrate Technologies- Organic, Embedding and Glass	Session 26: Process Innovation in Through-Via and Solder Interconnections	Session 27: Thermal Management and Material Solutions for High Performance 2.5D and 3D Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Kuldip Johal** **MKS Instruments** **Email: kuldip.johal@mks.com** **Markus Leitgeb** **AT&S AG** **Email: m.leitgeb@ats.net**	**Session Co-Chairs** **Vempati Srinivasa Rao** **Institute of Microelectronics A*STAR** **Email: vempati@ime.a-star.edu.sg** **Wei Zhou** **Micron Technology, Inc.** **Email: zhouwei@micron.com**	**Session Co-Chairs** **Dwayne Shirley** **Marvell Semiconductor, Inc.** **Email: shirley@ieee.org** **Ivan Shubin** **Raytheon Technologies** **Email: ishubin@gmail.com**
1. 9:30 AM - Copper Redistribution Layer (Cu-RDL) CPI Reliability Performance for Advanced Si Package With Coreless Substrate Kuo-Chin Chang, Chieh-Hao Hsu, Wei-Hsiang Tu, Tai-Shen Yang, Kuan-Cheng Peng, Hung-Chi Wu, Mirng-Ji Lii, Kathy Yan – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Deep Via and Trench Etching of Low CTE Glass Package Substrate Using SF6, NF3 and H2O Based NLD Plasma Process*** Yasuhiro Morikawa – ULVAC, Inc.; Srinivas Tadigadapa – Northeastern University	***1. 9:30 AM - Optimized TIM1 Solution for Large 2.5D HPC Packages Using Silicone Matrix Containing Liquid Metal Materials*** Po-Yao Lin, Kevin Lai, Yanling Huang, Han-wen Lin, JS Paek, Max Wu – Intel Corporation
2. 9:50 AM - Fully Encapsulated Fine Pitch Dual Damascene Organic RDL With Low Dk Df Photosensitive Polyimide and Its Reliability Minhua Lu – IBM Corporation; Joyce Liu, Peter Sorce, Andrew Giannetta, Michael Lofaro, Adele Pacquette, Michelle Hofman, David Rath – IBM Research	***2. 9:50 AM - Development of Straight, Small-Diameter, High-Aspect Ratio Copper-Filled Through-Glass Vias (TGV) for High-Density 3D Interconnections*** Ye Yang, Shuhang Lyu, Tiwei Wei – Purdue University; James Chien – Taiwan Foresight Co. Ltd.	***2. 9:50 AM - Novel Fabrication of Alumina Nanowires and Their Integration Into Alumina Nanowire, Membranes and Aerogels-Epoxy Composites for Enhanced Thermal Management in 2.5D/3D Semiconductor Packaging*** Zihao Lin, Wenbin Fu, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology
3. 10:10 AM - A Comparative Study on Power Delivery Network (PDN) Using Several Capacitor-Embedded Substrates for Next Generation Power Supply Applications Shuhei Yamada, Yuuki Yabuhara, Akitomo Takahashi, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.	***3. 10:10 AM - Metallization of Helium Tight and Thermo-Mechanically Reliable Through Glass Vias (TGV) by Conformal Pinched Via (CPV) Approach*** Mandakini Kanungo – Corning, Inc.; Rajesh Vaddi, Chukwudi Okoro, Scott Pollard, Prantik Mazumder – Corning Research and Development Corp.	***3. 10:10 AM - Characterization of PVD Backside Metal Adhesion for Improved Thermal Management in Heterogeneous Integration*** Carl Drechsel, Patrik Carazzetti, Eleftherios Stampolis, Roland Rettenmeier – Evatec AG; Ole Hoelck, Marcus Voitel, Friedrich Mueller, Karl-Friedrich Becker – Fraunhofer IZM
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Embedded Vertical Power Delivery Network Including Voltage Regulator for Over-1kW FC-BGA Based on 1.4 mm Thick-Core Organic Substrate Heeseok Lee – Samsung Electronics Co., Ltd.	***4. 11:15 AM - A Novel Approach to Ultra-Low Temperature Interconnection: Double-Sided SLID Process Using SAC BGAs and Off-Eutectic SnBiIn Paste*** Hafiz Waqas Ali, David Danovitch, Dominique Drouin – University of Sherbrooke; Divya Taneja – IBM Canada, Ltd.	***4. 11:15 AM - Newly Developed Low Df and Low CTE Material With High Thermal Stability for Organic Integration Board*** Shunsuke Tonouchi, Yuji Sakurazawa, Ayaka Takeguchi, Keiichi Kasuga, Hiroshi Shimizu, Shuji Gozu, Yukio Nakamura, Yusuke Sera – Resonac Corporation
5. 11:35 AM - Glass Core Substrate Versus Organic Core Substrate John H. Lau, Ning Liu, Mike Ma, TJ Tseng – Unimicron Technology Corp.	***5. 11:35 AM - Microwave and Cryogenic Performance of Solder Ball Jetted Flip-Chip Interconnect for Superconducting Quantum Devices for Radio Astronomy*** Max Behrens, Mohamed Aniss Mebarki, Alexei Pavolotsky, Denis Meledin, Francois Joint, Victor Belitsky, Vincent Desmaris – Chalmers University of Technology	***5. 11:35 AM - Thermal Management of Nano-TSVs in Advanced BS-PDN: A Comparative Study of AlN and Oxide Dielectrics for Heat Dissipation Efficiency*** Ya-Ching Tseng, Huicheng Feng, Gongyue Tang, Hong Yu Li – Institute of Microelectronics A*STAR
6. 11:55 AM - Development of Glass Core Build-Up Substrate With TGV Masahiro Sunohara, Jun Yoshiike, Hiroshi Taneda, Yoko Nakabayashi, Noriyoshi Shimizu – Shinko Electric Industries Co., Ltd.	***6. 11:55 AM - Formic Acid Vapor Assisted Fluxless TCB for Advanced Packaging- a Key Enabler for Ultra-Fine Pitch and High-Density Interconnects*** Adeel Bajwa, Suleman Ayub, Tom Colosimo, Matt Wasserman, Bob Chyla – Kulicke and Soffa Industries, Inc.	***6. 11:55 AM - Mold Underfill Process With Sheet Molding Compound for Full-Reticle Size Dies With Single-Digit Micrometer Gaps*** Yuki Sugiura, Daisuke Mori, Katsushi Kan – Nagase ChemteX Corporation
7. 12:15 PM - High-Aspect-Ratio, 6-µm-Diameter Through-Glass-Via Fabrication Into 100-µm-Thick ENA1 by Dry Laser Micro-Drilling Process Toshio Otsu, Tsubasa Endo, Hiroharu Tamaru, Yohei Kobayashi – University of Tokyo; Yoichiro Sato, Akihiro Shibata – AGC, Inc.	***7. 12:15 PM - Enhancing Wafer-Level Cu-Solder Bonding: A Fluxless Approach With Cu-Selective Passivation Coating*** Kevin Antony Jesu Durai, Dinesh Kumar Kumaravel, Khanh Tuyet Anh Tran, Oliver Chyan – University of North Texas	***7. 12:15 PM - Low Dk/Df Siloxane Hybrid Laminates for Advanced Packaging Substrate*** Seung-Mo Kang, Hyungshin Kweon, SungHun Park, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology

Program Sessions: Friday, May 30, 9:30 a.m. - 12:35 p.m.

Session 28: Reliability of Heterogeneous Integrated Packages	Session 29: Advances in Additive Manufacturing, Wearable and Medical Technologies	Session 30: Simulations on Advanced Package Processing - Hybrid Bonding, Chip Stacking and Wafer-to-Wafer
Committee: **Applied Reliability**	**Committee:** **Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Keith Newman** **Advanced Micro Devices, Inc.** **Email: keith.newman@amd.com** **Scott Savage** **Medtronic, Inc.** **Email: scott.savage@medtronic.com**	**Session Co-Chairs** **Tengfei Jiang** **University of Central Florida** **Email: tengfei.jiang@ucf.edu** **Chukwudi Okoro** **Corning Research and Development Corp.** **Email: okoroc@corning.com**	**Session Co-Chairs** **Chang-Chun Lee** **National Tsing Hua University** **Email: cclee@pme.nthu.edu.tw** **Yong Liu** **ON Semiconductor** **Email: Yong.Liu@onsemi.com**
1. 9:30 AM - A Procedure for Evaluating the Chiplet-Module-System Interaction of a 2.5-D Package Under Board-Level Reliability Test Condition Jing-An Huang, Tz-Cheng Chiu, Zhi-Yin Huang – National Cheng Kung University	***1. 9:30 AM - Rapid Prototyping of Advanced Packaging Using 3D-Printed Fanout Interposer Substrates With Diagonal Through-Holes*** Haksoon Jung, Yurim Choi, Jimin Kwon – Ulsan National Institute of Science & Technology; Nahyeon Kim – Ulsan National Institute of Science and Technology; Hyunjin Park – Korea Research Institute of Chemical Technology	***1. 9:30 AM - Atomistic Modeling of Interfacial Cracking in Copper-to-Copper Direct Bonding*** Shengfeng Yang – Purdue University
2. 9:50 AM - Influence of Passivation Layer on Electromigration Lifetime of Fine-Pitch Cu RDL Adrija Chaudhuri, Johannes Jaeschke, Astrid Gollhardt, Hermann Oppermann – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin	***2. 9:50 AM - Fully Printed Pressure Sensor Array for Soft Robotics*** Sara Lieberman, Riadh Al-Haidari, Babatunde Falola, Mark Poliks – Binghamton University; Deepak Trivedi, Pei-Hsin Kuo – GE Global; Felippe Pavinatto – GE Aerospace Research; Jack Ly – BlueHalo	***2. 9:50 AM - Crystal Plasticity-Based Modeling and Experimental Validation of the Influence of Microstructures and Grain Boundary Junction Types on the Cu-Cu Bonding Interface.*** Jae-Uk Lee, Hyun-Dong Lee, Sung-Hyun Oh – Sungkyunkwan University; Sung-Ho Park, Won-Seob Cho, Yong-Jin Park – BASF Korea; Alexandra Haag, Soichi Watanabe – BASF
3. 10:10 AM - Fabrication Optimization and Reliability Study of Hyper RDL (HRDL) Interposer for Advanced Packaging and Heterogeneous Integration Chun-Ta Li, Yu-Lun Liu, Tzu-Han Sun, Wen-Tzu Tsai, Mu-Ping Hsu, Yuan-Chiu Huang – National Yang Ming Chiao Tung University; Chien-Kang Hsiung – National Yang Ming Chiao Tung University / Applied Materials Inc; Yu-Tao Yang – MediaTek USA, Inc.	***3. 10:10 AM - Direct Digital Manufacturing for Laser-Drilled Vias in Multilayer Glass Additively Manufactured Electronics*** Sam LeBlanc, Jason Benoit – nScrypt; Kenneth Church – Sciperio	***3. 10:10 AM - Thermal Resistance at the Hybrid Bonding Layer in 3D-Stacked Dies for Electronic Packaging With FDTR*** Xavier Brun, Seyed Hadi Zandavi, Je-Young Chang – Intel Corporation; Aarom Schmidt – Fourier Scientific LLC
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - The Influence of Full IMC Structure on Micro-Bump Electromigration Performance Chung-Yu Chiu, Jui-Shen Chang, Tzuan-Horng Liu, Chen-Nan Chiu, Yao-Chun Chuang, An-Jhih Su, Ryan Lu – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 11:15 AM - Design and Fabrication of Bendable Double-Layer RDL Metallization Based on FOWLP for In-Mold Flexible Hybrid Electronics (iFHE)*** Chang Liu, Jiayi Shen, Atsushi Shinoda, Han Zhang, Tetsu Tanaka, Takafumi Fukushima – Tohoku University	***4. 11:15 AM - Tailoring Sintering Pressure to Optimize Nanoparticle Connectivity and Mechanical Strength in Cu-Based Interconnects*** Leiming Du, Weiping Jiao, G. Q. (Kouchi) Zhang – Delft University of Technology; Jiajie Fan – Fudan University
5. 11:35 AM - First Proof of 3D-IC Power Plane Defect Localisation via Frequency Domain Spatial Heat Mapping Zhansen Shi, Lucas Lum, Yeow Kheng Lim – National University of Singapore; Bernice Zee, J.M. Chin – Advanced Micro Devices (Singapore) Pte Ltd	***5. 11:35 AM - FlexPower II : Integration of Flexible Battlet Interdigitated Battery and FlexTrate™ for Wearables*** Mansi Sunil Sheth – UCLA -Center for Heterogeneous Integration and Performance Scaling (CHIPS); Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)	***5. 11:35 AM - Wafer Substrate Impact on Direct Wafer-to-Wafer Bonding Process*** Nathan Ip, Yuhai Xiang, Xuemei Chen – Tokyo Electron America, Inc.; Norifumi Kohama, Kimio Motoda – Tokyo Electron Kyushu, Ltd.
6. 11:55 AM - Advanced Thermal Management for High Power HPC, AI Nokibul Islam, JoonYoung Choi – STATS ChipPAC, Ltd.; Choong Kooi Chee – Marvell Technology, Inc.	***6. 11:55 AM - Point of Care Device for Early Detection of Polycystic Ovary Syndrome (PCOS)*** Siti Rafeah Mohd Rafei, Musafargani Sikkandhar, Karen Yanping Wang, Ramona Damalerio, Norhanani Jaafar, Ming-Yuan Cheng – Institute of Microelectronics A*STAR	***6. 11:55 AM - Advanced Packaging Techniques: Hybrid Numerical and Experimental Analysis of Underfill Flow in Fine Pitch Multi-Chip Modules*** Srikar Vallury, Ching-Kai Chou, Zi-Hsuan Wei Wei, Wei-Yu Lin, Yu-En Liang – CoreTech System (Moldex3D); Kazuki Noguchi – Sanyu Rec Co., Ltd.; Leo Shen – Moldex3D Northern America, Inc.
7. 12:15 PM - Study on Board-Level Reliability of 100x100 mm2 Large Glass Packages: Warpage, Thermo-Mechanical Reliability, and Parameter Envelope for High-Performance Computing Applications YongWon Lee, Kaushik Godbole, Suresh K. Sitaraman, Hyunggyu Park, Kyoung-Sik Moon, Muhannad Bakir – Georgia Institute of Technology	***7. 12:15 PM - Design, Materials Selection, and Assembly Process for a CMUT-Based Handheld Ultrasound Probe Head: Overcoming Development Challenges*** KM Rafidh Hassan, Gaurav Mehrotra, Hazel Caballero, Steven Lee – Renesas Electronics America; Karim Allidina, Tommy Tsang, Mohannad Elsayed, Hani Tawfik – MEMS Vision International, Inc.	***7. 12:15 PM - Simulation Analysis of Edge Dot-Void Formation and Edge Roll-Off Effects in Wafer-to-Wafer Bonding*** Sunghwan Kim, Youngsoo Kim, Geun-Myeong Kim, Minyeong Je, Yoon-Suk Kim – Samsung; Cheolmin Shin, Kyu-Ha Lee, Dongchan Lim – Samsung Electronics Co., Ltd.

Program Sessions: Friday, May 30, 2:00 p.m. - 5:05 p.m.

Session 31: Automotive Power	Session 32: Design, Materials, Metrology & Standards for Next Generation Interconnections	Session 33: Innovative Interconnects and Through Via Technology for 3D Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Mike Gallagher** **DuPont Electronic Materials** **Email: michael.gallagher@dupont.com** **Albert Lan** **Applied Materials, Inc.** **Email: Albert_Lan@amat.com**	**Session Co-Chairs** **Bernd Ebersberger** **Infineon Technologies AG** **Email: bernd.ebersberger@infineon.com** **Yoshihisa Kagawa** **Sony** **Email: Yoshihisa.Kagawa@sony.com**	**Session Co-Chairs** **Qianwen Chen** **Broadcom, Inc.** **Email: wendy.chen@broadcom.com** **Bo Song** **HP Inc.** **Email: bo.song@hp.com**
1. 2:00 PM - Development of a Micro Flake-Based Copper Sinter Paste for Low Temperature Sintering Rocky Kumar Saha, Hamza Bin Aqeel, Gordon Elger – Technical University of Applied Science Ingolstadt; Thomas Rubenbauer – Schlenk; Jens Heilmann, Bernhard Wunderle – Chemnitz University of Technology	***1. 2:00 PM - Process Development and Microstructure Characterization of Small-Diameter (< 3 µm), Cobalt-Filled Through-Silicon Vias (TSV) for High-Density 3D Chip Stacking*** Xinyi Zhang, Shuhang Lyu, Tiwei Wei – Purdue University	***1. 2:00 PM - Direct Bonding of Porous Cu Bumps Fabricated Using Gas Treatment of Cu-Sn Bumps*** Zilin Wang, Wenjie Zhao, Ziqing Wang, Zheyao Wang – Tsinghua University
2. 2:20 PM - Development and Evaluation of a Novel Package for 650V Bi-Directional GaN Switch Wenli Zhang, Jiawen Wen – GaNext Technology Co. Ltd.; Donghyo Jeon, Shoonho Kwon – HANA Microelectronics Public Co. Ltd.	***2. 2:20 PM - Are Voids Restricted to Cu-Cu bonding Interface? Truth Revealed by CEY-Scanning Transmission X-ray Microscopy*** Murugesan Mariappan – NICHe	***2. 2:20 PM - Enabling 10 µm Die-to-Die Pad Pitch in Flexible Fan-Out With TrueAdapt™*** Golam Sabbir – CHIPS UCLA; Subramanian Iyer, Jui-Han Liu – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS); Henry Sun – University of California, Los Angeles
3. 2:40 PM - Novel Metal Based Thermal Interface Materials for Flip Chip Ball Grid Array Packages Karthik Visvanathan, Arifur Chowdhury, Sachin Deshmukh, Sergio A Chan Arguedas, Krishna Vasanth Valavala, Luisa Cabrera Maynez – Intel Corporation	***3. 2:40 PM - Ultra-Fast Cu/Polymer Hybrid Bonding With Electroless Passivation Layer for Cost-Effective High I/O Interconnection Stacking*** Yu-Lun Liu, Tzu-Yu Chen, Chun-Ta Li, Jia-Rui Lin, Yi-Hsuan Chen – National Yang Ming Chiao Tung University; Kazuaki Ebisawa, Makiko Irie, Ya-Chien Chuang – Tokyo Ohka Kogyo Co., Ltd.	***3. 2:40 PM - Novel Thick Dry Film Photoresist and Process Optimization for High-Aspect Cu Pillar Patterning*** Hajime Furutani, Junya Kosaka, Masatoshi Ikemi, Masayuki Kishino, Masaya Toba – Asahi Kasei Corporation
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Study of the Optimal Cu Core Size Based on Surface Evolver for Solder Bridge and HiP Free of Large PBGA Package Hojin Seo, Junho Lee, Insik Han – Samsung Electronics Co., Ltd.	***4. 3:45 PM - X64 UCIe Chiplet Interconnection at 32 GT/s on a Silicon Core Substrate*** Steven Verhaverbeke, Seann Ayers, Shivkumar Chiruvolu, Han-Wen Chen – Applied Materials, Inc.; Farhang Yazdani – BroadPak Corporation	***4. 3:45 PM - Study of 2 x 4 µm Pitch Capsule Shaped TSVs and 2 µm Pitch TSVs in WoWoW Integration*** Masaki Haneda, Takuhiro Miyawaki, Yukari Fukumizu, Kosei Kubota, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation; Yoshihisa Kagawa – Sony
5. 4:05 PM - Localized Formation of Non-Conductive Paste (NCP) on 11 µm Diameter Bumps, Applied to 20 µm Pitch Chiplet Chip-on-Wafer (CoW) Bonding Jungho Shin, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ji-Eun Jung, Ga-Eun Lee – Electronics and Telecommunications Research Institute	***5. 4:05 PM - Study of High-Density Optical Redistribution Layer Enabling Advanced Chiplet Edge Bandwidth Density on Active Optical Package Substrate*** Akihiro Noriki, Fumi Nakamura, Satoshi Suda, Tadashi Murao, Haruhiko Kuwatsuka, Takeru Amano – National Institute of Advanced Industrial Science and Technology	***5. 4:05 PM - Bottom-Up Electrodeposition of Small Diameter, High Aspect Ratio Nanotwinned Copper-Filled Through-Silicon Vias for Ultra High-Density 3D Integration*** Yuchen Bao, Shuhang Lyu, Tiwei Wei – Purdue University
6. 4:25 PM - Mechanical and Electrical Evaluation of Materials for High Temperature Additively Packaged IMU on 3D AlN Ceramic Substrates Mousa Al-Zanina, Erik Busse, Emuobosan Enakerakpo, Stephen Gonya, Mohammed Alhendi, Mark Poliks – Binghamton University; David Lin, Cathleen Hoel – General Electric Global Research	***6. 4:25 PM - A Study About Bonding Properties With Multilayer Porous Structures for Fine Pitch Interconnection*** Takuma Nakagawa, Daiki Furuyama, Takuma Katase, Sho Nakagawa – Mitsubishi Materials Corporation	***6. 4:25 PM - Dry Film Photo-Imageable Dielectric Enabling Glass Core Substrate TGV Filling and Build-Up*** Yaming Jiang, Patrick Huang, Jason Chuang, George Yen, Zhou Lu, Colin Hayes, Chris Gilmore, LiYen Lin – DuPont
7. 4:45 PM - Multi-Channel E-Mode AlGaN/GaN Trigate FinFET - Design Space Exploration and Optimization for Vertical Power Delivery With Embedded Power Converters Ayoub Sadeghi, Inna Partin-Vaisband – University of Illinois	***7. 4:45 PM - Massive Orthogonal Stacking Assembly IC Cube (MOSAIC) With Inductive Coupling for Exascale Memory Applications*** Masaya Kawano, Yuki Mitarai, Mototsugu Hamada – University of Tokyo; Hiroyuki Hashimoto, Takafumi Fukushima – Tohoku University; Hiroshi Hosokawa, Jumpei Fujikata – EBARA Corporation; Hiroshi Kikuchi – YAMAHA ROBOTICS HOLDINGS CO., LTD.	***7. 4:45 PM - Development of Via-First TSV and Backside Interconnect Process for Large-Scale Superconducting Quantum Annealing Circuits*** Naoya Watanabe, Yuuki Araga, Katsuya Kikuchi – National Institute of Advanced Industrial Science and Technology; Ayuka Morioka, Kunihiko Ishihara, Tomohiro Nishiyama – NEC Corporation

Program Sessions: Friday, May 30, 2:00 p.m. - 5:05 p.m.

Session 34: Reliability of Interconnects in Advanced Packaging	Session 35: High -Performance Antenna and RF Design	Session 36: Modeling Driven Packaging and Process Advancements
Committee: **Applied Reliability**	**Committee:** **Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Seung-Hyun Chae** **SK hynix Inc.** **Email: seunghyun1.chae@sk.com** **Yan Li** **Samsung Semiconductor, Inc.** **Email: yanli7274@gmail.com**	**Session Co-Chairs** **Harrison Chang** **Advanced Semiconductor Engineering, Inc. (US)** **Email: Harrison_Chang@aseglobal.com** **Sungwook Moon** **Samsung Electronics Co., Ltd.** **Email: sw2013.moon@samsung.com**	**Session Co-Chairs** **Christopher J. Bailey** **Arizona State University** **Email: christopher.j.bailey@asu.edu** **Suresh K. Sitaraman** **Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 2:00 PM - Impact of Current stressed SAC305 and Sn-Bi Interconnect Anode and Cathode Side Thermo-Mechanical Stability Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.; Young-Woo Lee, Hui-Joong Kim, Seul-Gi Lee – MK Electron Co., Ltd.; Choong-Un Kim – University of Texas, Arlington	***1. 2:00 PM - 3D Vertical Glass Stacking for 6G Communications - Interconnect Fabrication and Broadband Characterization*** Xingchen Li, Lakshmi Narasimha Vijay Kumar – Georgia Institute of Technology; Madhavan Swaminathan – Pennsylvania State University	***1. 2:00 PM - Overall Packaging Process Warpage Simulation and Experimental Validation of Large 2.3D Bridge Die Chip From Wafer Level to Packaging Level*** Jian Cheng, Liping Zhu – JCET Group Co. Ltd.
2. 2:20 PM - Toward a Comprehensive Understanding of Electromigration Under AC Loads Impacting Microstructure and Reliability of SAC Solder Interconnects Hariram Mohanram, Yiram Kim – United Test and Assembly Center, Ltd.; Choong-Un Kim – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.	***2. 2:20 PM - Multi-Disciplinary Design Optimization of High-Speed Ceramic LCCC Package Through Automated Simulation*** Li Jiang, Guangxu Li, Jie Chen, Rajen Murugan, Muhammad Khan – Texas Instruments, Inc.	***2. 2:20 PM - Multi-Layer Sequential Fabrication and Mechanics-Based Model of Glass-Core Packages With Embedded Dies*** Alexander King, Kyoung-Sik Moon, Mohan Kathaperumal, Muhannad Bakir, Suresh K. Sitaraman – Georgia Institute of Technology
3. 2:40 PM - Deterioration of Electromigration Reliability in Microbumps due to Severe Side Wall Wetting Yifan Yao, Yuanxing Duan, Yuxuan An, K. N. Tu, Yingxia Liu – City University of Hong Kong; Songpeng Zhao, Yuzheng Guo – Wuhan University	***3. 2:40 PM - On-Chip Shoelace Fully Integrated Inductor*** Yushu Zhao, Yousef Safari – McGill University; Boris Vaisband – University of California, Irvine	***3. 2:40 PM - A Novel Fracture Mechanics Technique on Studying Passivation Crack Behavior for Advanced Si Package With Aluminum Redistribution Layer (Al-RDL) Routing*** Kuo-Chin Chang, Shao-Chen Tseng, Chieh-Hao Hsu, Wei-Hsiang Tu, Chang-Fu Han, Jyun-Lin Wu, Mirng-Ji Lii, Kathy Yan – Taiwan Semiconductor Manufacturing Company, Ltd.
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Prediction of Effect of Bi-Addition in SnAgCu Solders on High Strain Rate Properties Pradeep Lall, Vishal Mehta, Mrinmoy Saha, Jeffrey Suhling – Auburn University; David Locker – US Army	***4. 3:45 PM - Terahertz 300GHz Antenna in Package for 6G applications*** Mei Sun, Teck Guan Lim – Institute of Microelectronics A*STAR	***4. 3:45 PM - Interface Reliability of Advanced Packaging Under Sequential Stresses of High-Temperature and Temperature-Humidity in Automotive Environments*** Pradeep Lall, Padmanava Choudhury, Aathi Pandurangan, Madhu Kasturi, Jeffrey Suhling – Auburn University
5. 4:05 PM - High Precision Work-of-Adhesion Measurements Done Through In-Situ Wedge Testing Alex Wang, Carl Thompson, Cem Tasan – Massachusetts Institute of Technology	***5. 4:05 PM - Integration of D-Band 140 GHz III-V Components Transceiver in Embedding PCB-Based Technology*** Tekfouy Lim, Stefan Kosmider, Kavin Senthil Murugesan, Thi Huyen Le, Marius Van Dijk, Johannes Jaeschke, Ivan Ndip, Ulrike Gasnesh – Fraunhofer IZM	***5. 4:05 PM - Design and Manufacture of Integrated Passive Device in Coreless Package Substrates for Power Applications.*** Sylvester Ankamah-Kusi, Guangxu Li, Jonathan Noquil, Ayi Calma, Rajen Murugan, Jason Colte – Texas Instruments, Inc.
6. 4:25 PM - Challenges and Solutions for Measuring Copper-Polymer Interfacial Adhesion Strength in RDL of Advanced Packaging Wu-Lung Wang, Hsin-Chih Shih, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chin-Li Kao, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)	***6. 4:25 PM - Designing Antennas and RF Components at 110-330 GHz Using IPD Technology*** Muhammad Ibrahim, Kimmo Rasilainen, Aarno Parssinen, Marko E. Leinonen – University of Oulu; Jan Saijets, Pekka Rantakari – VTT Technical Research Centre of Finland	***6. 4:25 PM - Simulation of Mechanical Cu Pad Expansion Mechanism and Measures to Increase Expansion*** Takaaki Hirano, Taichi Yamada, Yuriko Yamano, Naoki Komai, Takumi Onodera, Yukako Ikegami, Shoji Kobayashi, Yoshiya Hagimoto – Sony Semiconductor Solutions Corporation
7. 4:45 PM - Study of Die Attach and Solder Mask Material Property Impacting BGA Substrate Reliability Performance for Automotive Application Stephen Lee, Jasmine Lim, Ryan Zhang, Abdullah Fahim, Yaxiong Chen, Sharan Kishore, Jetse De Witte, Tu-Anh Tran – NXP Semiconductor, Inc.	***7. 4:45 PM - G-Band Micromachined 4x1 & 8x1 Crossed Linear Array Antennas*** Alexander Wilcher, Shreya Sahai, Payman Pahlavan, David Arnold, Yong-Kyu Yoon – University of Florida; Alex Phipps, Jia Chieh – Naval Information Warfare Center	***7. 4:45 PM - Assessing Solder Joint Reliability Under Multi-Shock Loading by a Cohesive Zone Approach With Irreversible Damage Progression*** Krishna Kiran Talamadupula, Mohd Syazwan Abdul Samad, Chun-Sean Lau, Bo Yang – Western Digital Corporation

Wednesday May 28

Session 37: Interactive Presentations 1

10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs
Joshua Dillon
Marvell Technology, Inc.
Email: jdillon@marvell.com

Shiyao Lin
University of Texas, Arlington
Email: shiyao.lin@uta.edu

Saikat Mondal
Intel Corporation
Email: saikat.mondal@intel.com

Mark Poliks
Binghamton University
Email: mpoliks@binghamton.edu

Study of Interfacial Fracture Mechanics in IC Packaging Under Thermal Cycling
Marco Rovitto, Samuele Zalaffi – ST Microelectronics

Temperature Experiments For A 3D-Printed Encapsulated Thermal MEMS Wind Sensors Under Low Pressure
Sicun Duan, Zongyuan Cao – Southeast university; Zhenxiang Yi, Ming Qin, Qing-An Huang – Southeast University

Deep Learning Enhanced Thermal Simulation for Efficient Semiconductor Layout Design Using Thermal Twin
Bin He, Gongyue Tang – Institute of Microelectronics A*STAR

Architecting the Thermal Dissapation and Power Delivery for Large-Scale Systems and Experimental Demonstration of the Segmented Cooling for Silicon Thermal Dielets With a Power Density of 1 W/mm2
Haoxiang Ren, Ben Yang, Naarendharan Sundaram, Timothy Fisher, Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS); Dongkai Shangguan – Thermal Engineering Associates, Inc.

Machine Learning-Driven Warpage Prediction for Advanced Package
Pengcheng Yin, Yangyang Lai, Junbo Yang, Seungbae Park – Binghamton University

Enhanced AEC Qualification of Groundbreaking 5nm AI Processor With Liquid Cooling for Level 4 Autonomous Driving
Fen Chen, Qing Yang, Jie Liu, Daniel Dsouza, Howard Davidson, Daniel Beckmeier, Elliott Wu, Jitu Khare – Cruise LLC

Corrosion Analysis of the Electrode Coating in Film Capacitors for Power Electronics Applications
Sandy Klengel, Robert Klengel, Bolko MÃ¼hs-Portius – Fraunhofer IMWS

Electromigration Lifetime Improvement of Ball Grid Array Solder Joints for High Performance Computing Applications
Cameron Drewes, Andrea Molina Moreno, Miftahul Nabila, Kaitlyn Munoz, Tengfei Jiang – University of Central Florida; Jeng Hau Huang – National Taiwan University; Omar Ahmed – Juniper Networks

Influence of Cycling Induced Damage on the Anand Model Parameters of SAC305 Lead-Free Solder
Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Omma Sumaiya, Jeffrey Suhling, Pradeep Lall – Auburn University

Low Temperature Solder Reliability Study for Photonics Packages
Nokibul Islam – STATS ChipPAC, Ltd.; Wallace Zhong, Cheng Yang – JCET Group Co. Ltd.

Influence of Doping on the Electromigration Performance of SAC Solder Alloys on BGA Components
Karthik Deo, Junbo Yang, Yangyang Lai, Dalei Yang, Seungbae Park – Binghamton University

Interconnect Reliability for Single-Step Sintered Die Stack
Nikhil Gupta, G. Q. (Kouchi) Zhang – Delft University of Technology; Sebastian Quednau – Nanowired GmbH; Sandy Klengel, Robert Klengel – Fraunhofer IMWS; Robin Simpson, Rene Poelma, Nick Liu – Nexperia

Comparison of Mechanical Response and Failure Characteristics of Selected SnAgCu-Based High-Temperature Solder Alloys
Sean Lai, Lijia Xie, David Halbrooks, John Blendell, Carol Handwerker, Ganesh Subbarayan – Purdue University; Morgana Ribas – MacDermid Alpha

Nanoindentation Based Methodology to Characterize the Adhesion Strength of Dielectric Bond Interfaces
Kris Vanstreels, Oguzhan O. Okudur, Yusuf Ozdemir, Mario Gonzalez, Eric Beyne – imec

Rapid Estimation of Anisotropic Thermal Conductivity in RDL for 2.5D Chiplet Designs
Sridhar Narayanaswamy, Jun Liu, Dingjie Lu, Wenzu Zhang, Richard Xian-Ke Gao, Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR; En-Xiao Liu – Institute of High Performance Computing A*STAR

A Novel Methodology for Characterizing and Validating Viscoelastic and Thermal Expansion Properties of Polymer Films
Hung-Yun Lin, Alexander Gamez – Texas Instruments, Inc.

Enhancing Reliability of Multi-Chip Modules by Using the Reinforcement Mechanisms of Side-Fill Technology
Chang-Chun Lee, Kai-Cheng Lin – National Tsing Hua University; Shen-Yu Yang, Chao-Chieh Chan, Chun-Wei Wang, Yu-Ju Chen – Wistron NeWeb Corporation

Characterization of Coupled Mechanical and Electrical Behavior of Porous Conductive PDMS-CNT/Graphene Based Foams Under Multidirectional Strain for Flexible/ Stretchable Electronics
Nicholas Ginga, Nathan Morgan – University of Alabama in Huntsville

Leveraging AI to Enable High-Fidelity Modeling of Substrate Thermo-Mechanical Behavior
Mitchell Page, Raquel de Souza Borges Ferreira, Edvin Cetegen, Doruk Aksoy, Nicholas Haehn – Intel Corporation

Artificial Intelligence-Based Warpage Prediction Model for Accelerating Thermo-Mechanical Simulation in Advanced Packaging
Jungeon Lee, Daeil Kwon – Sungkyunkwan University; Sun-Woo Lee, Taek-Soo Kim – Korea Advanced Institute of Science and Technology

Fast and Accurate Machine Learning Prediction of Back-End-Of-Line Thermal Resistances in Backside Power Delivery and Chiplet Architectures
Prabudhya Roy Chowdhury, Aakrati Jain, Dureseti Chidambarrao – IBM Research; Atsushi Ogino, Kartik Acharya – IBM Corporation

A Flexible and Scalable Thermal Test Vehicle Design for Electronics Cooling Solutions
Logan Horowitz, S. Tahmid Mahbub, Jiarui Zou, Robert Pilawa-Podgurski – University of California, Berkeley

An Effective 3D Thermal Network Integrated With Deep Learning for Improved Prediction of the 3D Thermal Properties of Complex Packaging Patterns
Jeong-Hyeon Park, Eun-Ho Lee – Sungkyunkwan University; Jaechoon Kim, Suk Won Jang, Sungho Mun – Samsung Electronics Co., Ltd.

Thermal Analysis and Design Guideline of Massive Orthogonal Stacking Assembly IC Cube (MOSAIC) With Bump Connection Enabling SoC-DRAM Direct Stacking
Hung-Chih Huang, Yuki Mitarai, Masaya Kawano, Mototsugu Hamada, Atsutake Kosuge – University of Tokyo

Raman and X-ray Imaging Based Thermo-Mechanical Characterization of Metal-Embedded Chip Assembly
Faharia Hasan Bhuiyan, Haohan Guo, Shubhra Bansal – Purdue University; Christina Seeholzer, Clayton Tu, John Carlson, Christopher Roper – HRL Laboratories, LLC

Thermal Modeling of IR Laser Debond With Inorganic Thin Film Release Layers
Thomas Sounart, Henning Braunisch, Paul Nordeen, Georgios Dogiamis – Intel Corporation

Applying GA-NN and Explainable AI for IC Packaging Warpage Optimization: A Case Study on Product Feature
Yan-Cheng Lin, Hung-Kai Wang, I-An Shou – National Cheng Kung University; Tang-Yuan Chen, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung – Advanced Semiconductor Engineering, Inc.

A Computational Framework to Predict the Maximum Possible Warpage Due to Package-to-Package Variations
Sharan Kishore – NXP Semiconductor, Inc.; Sandeep Shantaram – Independent Researcher; Bernd Buettner, Rene Kallmeyer – ANSYS, Inc.

Thermal Characterization of HBMs Integrated via Hybrid Bonding
Huicheng Feng, Yong Han, Gongyue Tang, Ling Xie, Vasarla Nagendra Sekhar – Institute of Microelectronics A*STAR

An Efficient Data Augmentation and Semantic Segmentation Framework for 3D Defect Detection of HBMs
Ramanpreet Singh Pahwa, Yang Yu, Jie Wang, Richard Chang, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong – Institute of Microelectronics A*STAR

Warpage Control Mechanism Study of Stiffener on AI Chip IC Packaging
Wei Gong, Shaoyin Guo, Shaojuan Yu, Cih Cheng, Berkan Alanbay, Babak Ashourirad, Taylor Gaines, Hailan Gong – Intel Corporation

Digital Design of Inter-Die Gap Fill Dielectric Film Processing for C2W Hybrid Bonding Using Finite Element Modelling
Sasi Kumar Tippabhotla, Mishra Dileep, Vasarla Nagendra Sekhar, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR

Mitigation of Wafer-to-Wafer Bonding Distortions Through Accelerated Simulations and Measurements
Oguzhan Orkut Okudur, Serena Iacovo, Shuo Kang, Deewakar Sharma, Mario Gonzalez, Eric Beyne – imec

Wednesday May 28

Session 38: Interactive Presentations 2

2:30 PM - 4:30 PM

Committee: Interactive Presentations

Session Co-Chairs
Karan Bhangaonkar
Google
Email: karanbhangaonkar@outlook.com

Frank Libsch
IBM Corporation
Email: libsch@us.ibm.com

Yoichi Taira
Keio University
Email: taira@appi.keio.ac.jp

Meenakshi Upadhyaya
Marvell Technology, Inc.
Email: mupadhyaya@marvell.com

Flexible Glass Electrical Characterization Using Aerosol Jet Printing
Ethan Kepros, Sambit Kumar Ghosh, Bhargav Avireni, Premjeet Chahal – Michigan State University

Bio-Packaging Development of a Wearable Fluidic Monitoring System for Improved Blood Glucose Management in Critically Ill Diabetic Patients
Ruiqi Lim, James Ven Wee Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

All-Silicon Multi-Chip Modules Based on Ultra-Thin Active Pixel Radiation Sensors
Ladislav Andricek – Semiconductor Laboratory of the Max Planck Society

Parasitic Extraction and Signal Integrity Analysis of Memristor-Based Crossbar Arrays for Neuromorphic Computing
Tahsin Shameem, Yi Zhou, Zohreh Salehi, Jose Schutt-Aine – University of Illinois; Hanzhi Ma – Zhejiang University

Development of a Wearable Sweat Sensor With a Paper-Based Microfluidic Channel for Dehydration Monitoring
Ramona Damalerio, Musafargani Sikkandhar, James Ven Wee Yap, Ruiqi Lim, Wei Da Toh, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

Broadband Optical Engine (BOE) System Integration by Wafer Level Process in HPC/AI Era
K.H. Lo, Y.R. Liang, T.W. Chen, Edward Lin, S.W. Liang, J.Y. Gene Wu, C.J. Wang, S.W. Lu – Taiwan Semiconductor Manufacturing Company, Ltd.

Cost-Effective Package Design for a Chiplet Interfaces on Organic Substrates Using Low Cost Design Rules
Chungju Kim, Taisik Yang, Yongseok Kang – LG Electronics

Signal and Power Integrity Optimization in 2.XD Packaging Using Novel RDL Bridge Die and Copper Pillar Interconnects for Wide I/O Applications
Youngeun Na, Soo Jeong Kim, Yeon Ji Shin, Hong Seok Kim, Sang Yeul Yeum, Jae-Sung Lim – HANA Micron, Inc.; SangYul Ha – Myongji University; Woojin Lee – Swevenz Inc.

Systematic Crosstalk Reduction Method for PAM4 Transmission on PCIe Lopro FPIO Connectors
Kewei Song, Yulin He, Haonan Wu, Milton Feng – University of Illinois

A Dual Mode BLS/LFR Microscope for Local Mechanical Property Imaging for Semiconductor Packaging Materials
Sebastian Engmann, Andrew Gayle, Christopher Soles, Chris Michaels – National Institute of Standards and Technology

Power Loss and Efficiency Characterization of SiC-Based Onboard Charger for Vehicle-to-Grid Application
Wen You Jhu, Hsien Chie Cheng – Feng Chia University; Yu Cheng Liu, Yan Cheng Liu, Chun Kai Liu, Tao-Chih Chang – Industrial Technology Research Institute

Packaging and Integration of Multifunctional Brain Computer Interface
Ziqi Jia, Yong-Kyu Yoon – University of Florida

A K-Band Circularly Polarized Antenna for Short Range Communication Applications
Moh'd Rasoul Masadeh, Amanpreet Kaur – Oakland University

Design Enablement Methodology for 3D Stacked RF Systems
Raju Mani, Dutta Rahul, Tengiz Svimonishvili, Mihai Rotaru – Institute of Microelectronics A*STAR

Quantifying Signal Return Path Imperfections on Eye Aperture in Die-to-Die Communication
Nicolas Izquierdo, Jiawei Zhang, Manoj Rafalia, Eric Foronda, Chan Qian, Gerardo Romo – Qualcomm Technologies, Inc.; Jaimeen Shah – Qualcomm India Pvt. Ltd.

Leveraging Advanced Packaging for IP Protection in Heterogeneous AI Hardware
Md Saad Ul Haque, Jingbo Zhou, Farimah Farahmandi, Mark Tehranipoor – University of Florida

A Compact Dual Band (28/39 GHz) 1x4 Antenna Array Design With Frequency Selective Surface-base (FSS) for 5G AiP Applications
Sheng-Chi Hsieh – Advanced Semiconductor Engineering, Inc. (US)

Large-Scale Spaceborne Deployable Active Phased Array Antenna Design Using Rigid Flexible Board for LEO Satellite Constellation
Hiroki Hayashi, Yasuto Narukiyo, Delburg Mitchao, Sena Kato, Takeshi Ota, Keito Yuasa, Wang Xiaolin, Jil Mayeda – Institute of Science Tokyo

A 6G Terahertz 256-Element Dual-Polarized MIMO Antenna Array With Low-Profile and Broadband
Xin Zhang, Yuxiang Zheng, Qidong Wang – Chinese Academy of Science-Institute of Microelectronics

Ultra Wideband Microstrip Antenna-in-Package With Meander-Slot Feeding and Parasitic Patch Arrays for n258 and n261 Dual Mode 5G NR Applications
Geun-uk Oh, Hanna Jang, Yong-Kyu Yoon – University of Florida

Time-Efficient Eye-Opening Estimation Method for High-Bandwidth Memory Interface Design With Equalizers
Joonhyun Kim, Yongho Lee – Samsung Foundry; Sungwook Moon – Samsung Electronics Co., Ltd.

Comprehensive Analysis for Signal Integrity Optimization Between Channel Loss and Reflection for High-Speed Interfaces
Zhu Chiheng, Il-Joon Kim, Yeseul Jeon, Mingda Dong, Linping Chen, Scott Powers – Qualcomm Technologies, Inc.

Machine Learning-Optimized Metasurface Matching Layer for Enhanced Deep Fat Sensing Using PDMS and FEP
Alfredo Bayu Satriya, Myles Joshua Tan, James Overmeyer, Yong-Kyu Yoon – University of Florida

Prediction of Cross Section Images and Optimization of Processes With Neural Network
Kohei Motojima, Hayato Sugiyama, Kaede Ameyama, Chiho Ueta – TAIYO HOLDINGS Co., Ltd.

AI-Driven Automatic Routing for UCIe Bridge With Heterogeneous Configurations in Advanced System-in-Package
Weiyang Miao, Chuan Seng Tan – Nanyang Technological University; Mihai Rotaru – Institute of Microelectronics A*STAR

Additive Manufacturing of Passive Electronic Components Using Aerosol Jet Printing and Reliability Tests for Aerospace Applications
Abdullah Obeidat, Emuobosan Enakerakpo, Erik Busse, Ashraf Umar, Mark Poliks – Binghamton University; Matthew Erdtmann, Adrian Pyke – Micro-Precision Technologies, Inc.

Novel Wireless PVDF-PEDOT:PSS/LIG Based Wearable Multimodal Sensing Platform
Reshmi Banerjee, Ghaleb Al-Duhni, Raj Pulugurtha – Florida International University

Micro-3D-Printed Antenna-in-Package Substrates With Quasi-Coaxial Through Vias
Nahyeon Kim – Ulsan National Institute of Science and Technology; Haksoon Jung, Yurim Choi, Yongwoo Lee, Jimin Kwon – Ulsan National Institute of Science & Technology; Yunsik Park – Korea Electronics Technology Institute; Seungyeon Koh, Hyeok Kim – University of Seoul

Advanced Characterization of the Cure Kinetics of a Liquid Encapsulant
Anthony Kotula, Ran Tao, Jianwei Tu, Young Jong Lee, Gale Holmes – National Institute of Standards and Technology

Surface Smoothing Based on Au Thin Film Transfer on Rough-Surface AlN Ceramic Substrates for Low-Temperature Bonding
Shintaro Goto, Kai Takeuchi, Shogo Koseki, Eiji Higurashi – Tohoku University

Capping Layers for Enhanced Crystallinity of Single-Crystal Germanium on Insulator in Monolithic 3D ICs
Yu-Ming Pan, Ching-Lin Chen, Hao-Tung Chung, Chiao-Yen Wang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Nien-Chih Lin, Chih-Chao Yang, Chang-Hong Shen – Taiwan Semiconductor Research Institute

Novel Optical Chiplet Structure Based on MCeP®
Yuji Furuta, Motoyuki Fukuhara, Tatsuaki Denda, Hisashi Kaneda, Tomoharu Fuji – Shinko Electric Industries Co., Ltd.

Micro-Optical Glass-Molded PIC-Couplers for Scalable Fiber-to-PIC Packaging in Co-Packaged Optics and Pluggable Form Factors
Jeremy Witzens, Bin Shen, Danny deKreij – aiXscale Photonics GmbH

Low-Cost Transceiver Integration for Next Generation Passive Optical Network
Tam Huynh, Cuong Tran, Tzu-Yung Huang, Yang Liu, K.W. Kim, Ting-Chen Hu, Rose Kopf, Mark Cappuzzo – Nokia Bell Labs

Enabling Heterogeneous Integration of Optoelectronic Circuits via Die-to-Die Low-Temperature Bonding With Ultrathin dielectrics.
Yi Xuan Yeo, BG Sajay, Leong Ching Wai, Ser Choong Chong, Andrew Whye Keong Fong, Hemanth Kumar Cheemalamarri – Institute of Microelectronics A*STAR

Thursday May 29

Session 39: Interactive Presentations 3

10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs
Rao Bonda
Amkor Technology, Inc.
Email: rao.bonda@amkor.com

Alan Huffman
L3Harris
Email: alan.huffman@ieee.org

Stephen Lee
NXP Semiconductor, Inc.
Email: Stephen.Lee@nxp.com

Kristina Young
Synopsys, Inc.
Email: kristina.youngfisher@gmail.com

Flux-Less Solder Ball Attachment Technology (FLAT): A Sustainable and Cost-Reducing Solution for Advanced BGA Assembly Using Laser-Assisted Bonding
Sehoon Yoo, Dongjin Kim, Seonghui Han, Sang Eun Han, Donggyu Choi – Korea Institute of Industrial Technology; Kwansik Chung, Eunchae Kim – Prinsol Co., Ltd

Technology for Forming Micro Vias Smaller Than 20 µm With Low Surface Roughness on Build-Up Films Using UV Nanosecond Laser Drilling and Plasma Desmearing
Nam Son Park, Tae-Young Lee, Sung Yong Kim, Sung Yoon Lee, Sang-a Yoon – Tech University of Korea; Mun Sang You, Geonhee Lee – SIMMTECH; Sehoon Yoo – Korea Institute of Industrial Technology

Fabrication of D-band (140 GHz) Broadband Antenna Using Quartz Glass on Silicon Hybrid Bonded Wafer With Cavity
Kentaro Tani, Naotake Okada, Masato Tokai, Shoichiro Yamaguchi, Jungo Kondo – NGK INSULATORS, LTD; Makoto Iwai – NGK INSULATORS, LTD./NGK Europe GmbH; Uwe Maaß, Alexander Gäbler, Ivan Ndip – Fraunhofer IZM

The Role of Surface Preparation and Bonding Parameters in Improving Hybrid Bonding Quality
Injoo Kim, Siye Lee, Jinho Jang, Minji Kang, Hyein Jin, Sungdong Kim – Seoul University of Science and Technology

Study of Sn Damascene Process for Novel Fine Pitch Microbump Bonding
Kosuke Yamashita – Fujifilm Electronic Materials Europe; John Slabbekoorn, Jaber Derakhshandeh – imec; Eric Turner – Fujifilm Electronic Materials U.S.A., Inc.

High Precision Large Reticle Thermo-Compression Bonding for Advanced Packaging for AI Era
Shripad Gokhale, Kartik Srinivasan, Shan Zhong, Anurag Tripathi – Intel Corporation

Electrical Performance of 2-Platen CMP Process for Hybrid Bonding Application With Conventional / nt-Cu and Low Temperature of SixNy / SixOy Dielectrics
Trianggono Widodo, Xavier Brun – Intel Corporation; Prayudi Lianto, Avery Tan, Joselyn Lie, Patrick Lim, Guan Huei See – Applied Materials, Inc.

IR Laser Debonding for Silicon Based Temporary Carrier Systems Enabling 2.5D and 3D Chiplet Integration Processes
Peter Urban, Simon Halas, Julian Bravin, Thomas Uhrmann, Markus Wimplinger – EV Group; FranÃ§ois Chancerel, John Slabbekoorn, Steven Brems – imec

Hydrophobic Barrier for Controlled Epoxy Keep-Out-Zone in Flip Chip Assembly
Paul Kim, John C. Decker, Xiying Chen, Ziyin Lin, Ifeanyi Okafor, Ke Geng, Yiqun Bai, Hsin-yu Li – Intel Corporation

Accelerating Root Cause Identification of Subtle Bonding Failures With Microwave Induced Plasma
Charles Odegard, Liv Bonin, Daniel Scott – Texas Instruments, Inc.; Yashan Peng, Jiaqi Tang, Mark McKinnon – JIACO Instruments; Kees Beenakker – Delft University of Technology

Wet-Chemical Cu Cleaning for Fine-Pitch Hybrid Bonding
Kohei Nakayama, Kenta Hayama, Fabiana Tanaka, Fumihiro Inoue – Yokohama National University; Sven Dewilde, Steven Deckers, Nancy Heylen, Harold Philipsen – imec; Yoichi Tanaka, Yusuke Okazaki, Nobuko Gan, Hideaki Iino – Kurita Water Industries Ltd.

Evaluation of Printed Materials for Flexible Hybrid Electronic (FHE) Interconnections and Packaging
Babatunde Falola, Riadh Al-Haidari, Udara Somarathna, Olya Noruz Shamsian, Bryan Cabrera, Mohammed Alhendi, Mark Poliks – Binghamton University; Gurvinder Singh Khinda – GE HealthCare

Rigid-to-Flex Interconnection for Flexible Hybrid Electronics Integration Using Anisotropic Conductive Adhesive
Riadh Al-Haidari, Babatunde Falola, Zhi Dou, Mark Schadt, Mohammed Alhendi, Mark Poliks – Binghamton University; Ekaterina Dvoretskaya, Andrew Stemmermann – SunRay Scientific, Inc.

A Mild Surface Activation Under Redox Gases Using Vacuum Ultraviolet Irradiation for Interconnection of Semiconductor Packaging
Shinichi Endo – Ushio, Inc.

Demonstration of a Fully Integrated, High Bandwidth, Active Flexible Connector for Large Area Computational Systems
Randall Irwin, Joanna Fang, Subramanian Iyer – University of California, Los Angeles

Warpage Engineering in C2W Hybrid Bonding Using Inter-Die Gap Fill Dielectrics for 2.5D/3D Integration
Mishra Dileep, Vasarla Nagendra Sekhar, Hemanth Kumar Cheemalamarri, Jun Wei Javier Ong, Sasi Kumar Tippabhotla, Chandra Rao B. S. S., Ser Choong Chong, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR

A High Throughput Low-Temperature Copper-Copper Thermal Compression Bonding Scheme Using Tin Passivation
Tanmay Konnur, Krutikesh Sahoo, Randall Irwin, Vineeth Harish – University of California, Los Angeles; Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

Advanced Face-To-Back CoW 2.0-µm Pitch Cu-Cu Hybrid Bonding Process for Three Layer-Stacked 3D Heterogenous Integration.
Akihiro Urata, Takahiro Kamei, Itsuki Imanishi, Masanori Chiyozono, Toru Osako, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation; Yoshihisa Kagawa – Sony

Process Approaches to Enable 200 °C Hybrid Bonding With SiCN Bond Layer and 0.5 µm Pitch
Kai Ma, Nikolaos Bekiaris, Eric J Bergman, Santosh Kumar Rath, Lei Xue – Applied Materials, Inc.; Taotao Ding, Barbara Weis, Gernot Probst – EV Group

High-Quality Cu µ-Joints by High-Throughput Contactless Hot-Isostatic-Pressure (HIP) Annealing for Chip-to-Wafer and Wafer-to-Wafer Hybrid Bonding
Murugesan Mariappan – NICHe

Fabrication of Panel-Level Redistribution Interposer With 1.5/1.5 Î¼m Multilayer Fine Wiring and Solutions to Issues of Miniaturization
Masashi Minami, Sachiko Matsushita, Sasakura Yuuna, Sadaaki Katoh – Resonac Corporation

Polyimide Fine Via and Trench Formation Based on Plasma Etching Technology for RDL Interposer
Fumito Otake, Kenta Doi, Yasuhiro Morikawa – ULVAC, Inc.

Growth of Nanovoids in Electroless Cu Layer of Micro-Via After Thermal Reliability Test
Masahiko Nishijima, Ming-Chun Hsieh, Zhang Zheng, Rieko Okumura, Aiji Suetake, Hiroyoshi Yoshida, Chuantong Chen, Katsuaki Suganuma – Osaka University; Hiroki Seto – Okuno Chemical Industries Co., Ltd.

Development and Characterization of Electrodeposited Tin-Indium Alloy Microbumps for Low Temperature Assembly
Tsvetina Dobrovolska, Martin Mack, Klaus Leyendecker – Umicore Galvanotechnik GmbH; Kevin Martin – Umicore EP USA; Aleksandar Radisic, Ehsan Shafahian, Zaid El-Mekki, Punith Kumar Mudiger Krishne Gowda, Jaber Derakhshandeh, Herbert Struyf – imec

Effect of Dimension on Thermal Expansion of Cu Pads in SiO2 Vias for 3D IC Fine-Pitch Hybrid Bonding
Pin-Lin Chen – National Yang Ming Chiao Tung University; Chih Chen – National Yang Ming Chiao Tung University

Impact of Temporary Substrates and Adhesives on Die-to-Wafer Overlay
Koen Kennes, Pieter Bex, Ye Lin, Samuel Suhard, Dieter H. Cuypers, Alain Phommahaxay, Gerald Beyer, Eric Beyne – imec

Patterning of Sub 1 µm Critical Dimension TSV for 2.5 µm pitch 2.5D/3D hybrid bonding Applications
Arvind Sundaram, Chandra Rao B. S. S. – Institute of Microelectronics A*STAR

Process Development, Challenges, and Strategies for Void-Free Multi-Chip Stacking in Hybrid Bonding Applications
Ser Choong Chong, Ling Xie, Vasarla Nagendra Sekhar, Mishra Dileep, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR

Ozone-Ethylene Radical Activation of SiCN/Cu Without Water Rinsing for Hybrid Bonding
Bungo Tanaka, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Murugesan Mariappan – NICHe; Soichiro Motoda, Tetsuya Nishiguchi – MEIDEN NANOPROCESS INNOVATIONS, INC.

Environmentally Friendly Cu Post Technology, Based on Laser-Assisted Bonding With Compression (LABC) and Fume-Free Laser Solder Paste for Advanced 3D Interconnections
Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Jungho Shin, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ho-Gyeong Yun – Electronics and Telecommunications Research Institute

Through GaN Via for 3D Heterogeneous Strata Integration
Jui-Han Liu, Haoxiang Ren, Cheng-Ting Yang, Boris Vaisband, Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

Microbump Interconnections Using Vertical Wire Technology for the Power Connections Between SoC and Substrate in Bridge Die-Based Packaging Platform
Ye-Jin Jang, Jin-Ho Lee, Yong-Gyu Jang, Sanggyu Jang, Na-Hyun Cho, Jin-Wook Jang – HANA Micron, Inc.

Novel Fault Isolation Methodology Applied on Nano-Scale Defect in Fine Line RDL for Advanced Fan-Out Package
Yi-Sheng Lin, Cheng-Hsin Liu, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung, Chun-Liang Kuo, Chia-Wen Hung – Advanced Semiconductor Engineering, Inc.

Thursday May 29

Session 40: Interactive Presentations 4

2:30 PM - 4:30 PM

Committee: Interactive Presentations

Session Co-Chairs
Mark Eblen
Kyocera International SC
Email: mark.eblen@kyocera.com

Li Jiang
Texas Instruments, Inc.
Email: l-jiang1@ti.com

Pavel Roy Paladhi
NVIDIA
Email: rpaladhi01@gmail.com

Ting Zheng
Marvell Technology, Inc.
Email: tzheng@marvell.com

Improving the Uniformity of Cu Deposition in Fan-Out Panel Level Package With FEM Simulation Model
Yung-Sheng Lin, Min-Yan Tsai, Mingtzung Kuo, Ling-yuan Chang, Ping-Feng Yang, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)

Lithography-Free Anisotropic Magnetoresistance Sensor-Based Rotational Speed Measurement System on PEEK With Integrated Electronics
Tim Nils Bierwirth, Marc Christopher Wurz – Leibniz University Hannover/ Institute of Micro Production Technology; Sebastian Bengsch, Michael Werner – Ensinger GmbH; Eike Christian Fischer – Freelancer

Effect of Plasma Etching and Color Difference of the Molding Compound Surface on Adhesion in Electromagnetic Shielding
Soichi Homma, Daichi Okada, Akihito Sawanobori, Susumu Yamamoto – KIOXIA Corporation; Hiroshi Nishikawa – Osaka University

Integrated Passive Devices in the Silicon Interconnect Fabric
Haoxiang Ren, Zoe Chen, Cheng-Ting Yang, Jui-Han Liu, Boris Vaisband, Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

Parametric Analysis of Thermo-mechanical Behavior for HBM in System-In-Package Configurations
Hyunggyun Noh, Wonhong Choi, Woongkee Kim, Gunhee Bae, Yumi Sim, Seungyeon Kim, Yuchul Hwang – Samsung Electronics Co., Ltd.; Yunsung Lee – Samsung Foundry

A Highly Reliable Filling Method for Package-on-Package Utilizing Epoxy Flux
Kisu Joo, Kyojin Hwang, Heeseok Lee – Samsung Electronics Co., Ltd.

Holistic Insight Into the Effects of Diverse Surface Modification Methods on Difficult-to-Bond Resin Materials
Akihiro Shimizu – Ushio, Inc.

A Novel Disaggregated Approach of Assembling Integrated Heat Spreader for Advanced Packages
Arifur Chowdhury, Jaclyn Avallone, Bamidele Falola, Taylor Gaines, Haowen Liu, Peng Li, Sergio A Chan Arguedas, Aravindha R Antoniswamy – Intel Corporation

Characteriation of FOWLP Process Using Temporary Bonding Material on Carrier With Very Low Die Shift
Tiffany Tang, Dieter H. Cuypers, Aldrin Vaquilar, Pieter Bex, Koen Kennes, Alain Phommahaxay, Eric Beyne – imec; Alice Guerrero – Brewer Science, Inc.

Wafer-to-Wafer Bonding With Saddle-Shaped Wafers
Shuo Kang, Serena Iacovo, Koen DâhavÃ©, Oguzhan Orkut Okudur – imec; Anton Alexeev, Thomas Plach, Taotao Ding, Markus Wimplinger – EV Group

Novel Packaging Platform Based on Bridge Dies With Top and Bottom I/O Connections on Standard Substrates
Jae-Sung Lim, Jin-Wook Jang, Sanggyu Jang, Yong-Nam Koh, Jayden Donghyun Kim – HANA Micron, Inc.

Advanced Resin Material Enabling Room-Temperature Bonding for WOW and COW 3DI Applications
Naoko Araki – Daicel Corporation; Tadashi Fukuda, Takayuki Ohba – Institute of Science Tokyo

Bond Wave Analysis of SiCN for Fine Pitch Hybrid Bonding
Fumihiro Inoue, Ryosuke Sato, Hayato Kitagawa – Yokohama National University; Atsushi Nagata, Yoshihiro Kondo – Tokyo Electron Kyushu, Ltd.; Kenichi Saito – Tokyo Electron, Ltd.; Jung Hwan Park, Chiwoo Ahn – SK hynix Inc.

Characterization of Interfacial Fracture Strength in Hybrid Bonded Wafers: A Novel Approach for High-Resolution Spatial Profiling
Sathya Raghavan, Nicholas Polomoff, Katsuyuki Sakuma – IBM Research; Qingyu Yang – University of California, Los Angeles

Laminate Materials With Excellent Co-Planarity and Dimensional Stability for Advanced 2.xD Package
Norihiko Sakamoto, Keita Johno, Kyousuke Sutou, Takayo Kitajima, Keitaro Iguchi, Yuji Mato – Resonac Corporation

Rapid Dendritic Amplification of Amino Groups on BN Surfaces for Enhanced Thermal Conductivity in Polymer Composites
Zihao Lin, Juwon Lim, Yu-Chieh Lin, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology

Preform-Type TIM1/1.5 Using Liquid Metal Reinforced With Z-Axis Oriented Carbon Fiber
Stephen Stagon, Robert Mone, Chunzhou Pan, Tao Huang, Seth Liyanage, Ethan Colburn, Nikhil Jani – Boston Materials

SiO2-Based Chiplet Reconstitution Technology for Multi-Height Chiplet Integration
Ashita Victor, Madison Manley, Muhannad Bakir – Georgia Institute of Technology

A New Wafer Level Package With Vertical Cu Post Stack for on-Device AI Solution
Woosang Jung, Sangkyu Lee, Haram Park, Eun Young Lee, Yieok Kwon, Myeonghan Bae, Jongyoun Kim, Wonkyung Choi – Samsung Electronics Co., Ltd.

Hybrid Substrates With Ultra-Large Organic Interposer for Heterogeneous Integration
Curry Lin, John H. Lau, Chun-Hung Chen, Kai-Ming Yang, Tim Xia, Cheng-Ta Ko, Bruce Puru Lin, Mike Ma – Unimicron Technology Corp.

Experimental Demonstration of High-Power Thermal Test Vehicle for Two-Phase Cooling for AI Datacenters, 5G RAN, and EDGE Compute Nodes
Yang Liu, Rishav Roy, David J. Apigo, Manohar Bongarala, Syed Faisal, Sarwesh Parbat, Todd Salamon, Mark Cappuzzo – Nokia Bell Labs

Cost and Performance Optimized Chiplet Package for Automotive and Edge Processors
Trent Uehling, Eli Tiffin, Nikhita Baladari, Gaurav Sharma, Stan Cejka – NXP Semiconductor, Inc.

Addressing Key Process Challenges in Developing High Aspect Ratio TSVs up to 15 With 1 µm Critical Dimension
Van Nhat Anh Tran, Arvind Sundaram, Ya-Ching Tseng, Nandini Venkataraman, Zeng Wei Heng, Binni Varghese, B.S.S. Chandra Rao – Institute of Microelectronics A*STAR

Development of High Thermal Conductance Wafer Bonding Interface With PVD Aluminum Nitride
Andrew Tuchman, Ayuta Suzuki, Christopher Netzband, Joshua Greklek, Rinus Lee, Ilseok Son – TEL Technology Center, America, LLC

Aluminum Nitride With Thermal Conductivity > 100W/mK as a Fusion Bonding Film for Backside Power Delivery
Michel Khoury, Liang Song, Chris Lee, Chengyu Liu, Maria Gorchichko, Kun Li, Tom Osterheld, Meng Zhu – Applied Materials, Inc.

Modeling and Validation of an Integrated Package Solution (iPaS) for Next Generation Power Supply Systems
Akitomo Takahashi, Shuhei Yamada, Yuuki Yabuhara, Masafumi Tanaka, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.

Development of Glass Core Substrates for Long-Term Reliability Under Thermal Stress
Koji Fujimoto, Takahiro Tai, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.

Electrolytic Copper Plating Process for Glass Substrates
Raihei Ikumoto, Shinji Tachibana, Hisamitsu Yamamoto, Yudai Kuramochi – C. Uyemura & Co., Ltd.

The Formation of Microvia With a Diameter of 3.5 µm and an Aspect Ratio of 3 in Ajinomoto Build-up Film® (ABF) Using KrF Excimer Laser Ablation
Kanta Wataji, Akira Suwa – Gigaphoton, Inc.; Yasufumi Kawasuji – Gigaphoton Inc; Daisuke Hironiwa, Eiji Baba, Ryo Miyamoto – Ajinomoto Fine-Techno Co., Inc.

Efficient Utilization of Different Kinds of Superelements for Thermo-Mechanical Reliability FE-Analysis of Chiplets
Mike Manuel Feuchter, Martin Hanke, Hanna Baumgartl – CADFEM GmbH

Mechanical Strength and Pad Cratering Risk Determination of High-Speed PCBs via Physical Testing and Numerical Simulation
Peng Su, Omar Ahmed, Aliasghar Dormohammadi, Leif Hutchinson, Bernard Glasauer – Juniper Networks

Friday May 30

Session 41: Student Interactive Presentations

10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs
Ibrahim Guven
Virginia Commonwealth University
Email: iguven@vcu.edu

Jeffrey Lee
iST-Integrated Service Technology, Inc.
Email: jeffrey_lee@istgroup.com

Wenhao (Eric) Li
Intel Corporation
Email: wenhao.li@intel.com

Jobert Van Eisden
MKS Instruments
Email: Jobert.van-Eisden@atotech.com

Characterization of the Mechanical and Thermal Properties of SAC+Bi Phases in Hybrid SAC/LTS Solder Joints
Souvik Chakraborty, Mahbub Alam Maruf, Golam Rakib Mazumder, Jeffrey Suhling, Pradeep Lall – Auburn University

Pick-and-Release: a Novel Contactless Bonding Method for Die Attachment
Ahmed Abdelwahab, Henk van Zeijl, Massimo Mastrangeli – Delft University of Technology; Remco van Hoorn, Hans Kuipers – ITEC Equipment

Assessment of Electromagnetic Board Level Shielding Using Continuous Carbon Fiber
Victor Mahaut, Wilson Maia – Thales Research & Technology; Tristan Dubois, Alexandrine Gracia – University of Bordeaux

3D Coupled Line Inductors With Through-Glass Vias for Compact Passive Circuit Integration in Glass Packages
Sojeong Kim, Young-Joon Kim – Gachon University; Jein Yu – Korea Electronics Technology Institute

Design, Fabrication and Characterization of a 3D-Printed Radix-Based Array Antenna for 5G mmWave Applications
Waleed Alshaibani, Abdullah Obeidat, Riadh Al-Haidari, Erik Busse, Stephen Gonya – Binghamton University; Jason Case, Joseph Iannotti, Felippe Pavinatto – GE Aerospace Research

Enhancing Runtime Security in Heterogeneous System-in-Package Through a Chiplet-Based Root-of-Trust
Amit Mazumder Shuvo, Md Sami Ul Islam Sami, Jingbo Zhou, Farimah Farahmandi, Mark Tehranipoor – University of Florida

Physics-Informed Neural Networks for SAM Image Enhancement With a Novel Physics-Constrained Metric for Advanced Semiconductor Packaging Inspection
Shajib Ghosh, Nitin Varshney, Antika Roy, Patrick Craig, Md Mahfuz Al Hasan, Sanjeev J. Koppal, Navid Asadi – University of Florida; Nelly Elsayed – University of Cincinnati

Thermo-Seal: A Multi-Layered Watermarking Scheme for On-Field IC Provenance Verification Using Camouflaged Thermal Signatures
Mohammad Shafkat Khan, Himanandhan Reddy Kottur, Nitin Varshney, Liton Kumar Biswas, Navid Asadizanjani – University of Florida; Stephan Larmann – InfraTec

Facile Fabrication for Flexible Pressure Sensor Using FDM-Type 3D Printing Technology
Junyoung Park, Hongyun So – Hanyang University

Electrospray Deposited Silver Films for Electromagnetic Interference (EMI) Protection on Insulating Targets
Emma Pawliczak, Paul Chiarot – Binghamton University

Scalable Metamaterial Antenna Arrays With Reduced Mutual Coupling for SWaP-Constrained Applications
Alexander Wilcher, Ariel Cerpa, Yong-Kyu Yoon – University of Florida; Shelby Nelson – Mosaic Microsystems

Heterogeneous Integration of Memristor Emulator for Low-Power Computing
Zohreh Salehi, Yi Zhou, Tahsin Shameem, Jose Schutt-Aine – University of Illinois; Hanzhi Ma – Zhejiang University

Microstructures and Joint Reliability of Sn-58Bi Solder Fabricated by Selective Intense Pulsed Light
Young-Joo Park, Geon-Joo Jeong – Korea Institute of Industrial Technology; Seung-Boo Jung – Sungkyunkwan University

Design and Verification of a UCIe-A Mimic Channel for Early-Stage Development of UCIe-Based Systems
Taesoo Kim, Taein Shin, Keunwoo Kim, Joungho Kim – Korea Advanced Institute of Science and Technology

Organic and Hybrid Nanoscale Films for Low Loss Direct Glass-Copper Metallization
Sai Saravanan Ambi Venkataramanan, Hyunggyu Park, Lakshmi Narasimha Vijay Kumar, Lila Dahal, Mohan Kathaperumal, Mark Losego – Georgia Institute of Technology

Optimization of Reflow Profile for Solder Thermal Interface Materials With an Inline Vacuum Oven
Piyush Kulkarni, Scott Schiffres – Binghamton University; Ali Davoodabadi – Universal Instruments Corp.

Characterization of Dielectric Materials Beyond Room Temperature Using the Lab-Developed Temperature Split Cavity (TSC) Method.
Arafat Hossain, Michael Marakovits, Steven Perini, Michael Lanagan – Pennsylvania State University

Chiplet Embedding in Glass-Core Package RDL
Hyunggyu Park, Muhannad Bakir – Georgia Institute of Technology

High-Frequency Multi-Chip RF Module Enabled by Fused-Silica Stitch-Chip Technology: RF and Interconnect Characterization
Zhonghao Zhang, Ting Zheng, Muhannad Bakir – Georgia Institute of Technology

Novel Technique of Universal Micropatterning for High Density Die Packaging
Alice Mo, Zachary Nelson, Luke Theogarajan – University of California, Santa Barbara

Void Formation Elimination in Ultra-Thin Au-Sn Solid-Liquid Interdiffusion Bonding Using Rapid Cooling Process for Advanced Packaging and MEMS Applications
Pei-Ru Lee – NationalÂ Yang MingÂ Chiao Tung University; Mu-Ping Hsu,, An-Yuan Hou, Wen-Wei Wu, Kuan-Neng Chen – National Yang Ming Chiao Tung University

Integration of Packaged Dies for Flexible FOWLP Using Low Temperature Solder Bonding On FlexTrateTM
Henry Sun, Guangqi Ouyang, Mansi Sheth – University of California, Los Angeles; Subramanian Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

Enhancing Reliability of 30 Î¼m-Pitch Interconnections by Optimizing Material Properties of Laser Non-Conductive Paste (LNCP) for Room Temperature Laser-Assisted Bonding With Compression (LABC)
Ga-Eun Lee, Young-Sung Eom, Gwang-Mun Choi, Ki-Seok Jang, Jungho Shin, Chanmi Lee, Jin-Hyuk Oh, Ji-Eun Jung – Electronics and Telecommunications Research Institute

Innovative High-Permeability Substrate Integrated Ferrite Inductors for Integrated Voltage Regulators
Rui Huang, Haowen Li, Xiaoling Shi, Nian-Xiang Sun – Northeastern University; Hwaider Lin, Hui Lu – Winchester Technology

Intermetallic Compounds (IMC) Growth Investigation, Kinetic Parameter Analysis and Relibility Evaluation of Indium Solder Metal for 3D Integration Packaging
Tassawar Hussain – KU Leuven; Jaber Derakhshandeh, Tom Cochet, Ehsan Shafahian, Prathamesh Dhakrasa, Eric Beyne, Ingrid De Wolf – imec; Aksel Goehnermeier – Carl Zeiss

High Aspect Ratio Spiral Inductor With Progressive Turn Widths for Embedded Power Converters
Rami Rasheedi, Inna Partin-Vaisband – University of Illinois

Efficient Scalable Thermoelectric Modeling of High-Frequency Cylindrical Interconnects for Heterogeneous Package Arrays
Mohamed Gharib, Inna Partin-Vaisband – University of Illinois

Hybrid Voltage Regulators for High Performance Computing: Analytical Models and Design Methodology
Salma Abdelzaher, Mohamed Gharib, Inna Partin-Vaisband – University of Illinois

Imaging Assisted Dual Sided Light Coupling Technique for Propagation Loss Estimation of Waveguide Interconnects
Abhinandan Hazarika, Brendan Roycroft, Muhammet Genc, Brian Corbett, Zhi Li – Tyndall National Institute

Direct-on-Chip Two-Phase Microjet Cooling With Surface-Enhanced Electrodeposited Microporous Structures
Keyu Wang, Ketan Yogi, Gopinath Sahu, Aaron Du, Tiwei Wei – Purdue University

Thermal Characterization and Benchmarking of Aluminum Ribbon Ceramic (ARC) Substrates in mmWave/RF Packaging Applications
Chenhao Hu, Kyoung-Sik Moon, Manos M. Tentzeris – Georgia Institute of Technology

Reliable Bonding Strength Measurement of SiCN/SiCN Films by Four-point Bending Methodology
Yun-Hsuan Chen, Pin-Syuan He, Yi-Chen Chung, Rou-Jun Lee, Chien-Yu Liu – National Yang Ming Chiao Tung University; Guan-Zhe You, Chang-Chun Lee – National Tsing Hua University; Chih Chen – National Yang Ming Chiao Tung University

High-Power Vapor Chambers With Hierarchical Dendritic Wick Structures for High-Performance Computing Systems
Chao-Yang Chiang, Po-Hsun He, Chien-Neng Liao – National Tsing Hua University; Yu-Hsiang Chang, Hung-Hsien Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung – Advanced Semiconductor Engineering, Inc.

Advanced Constitutive Modeling of Epoxy Molding Compound for Fatigue Life Prediction
Dajeong Yun, Seungwoo Kim, Geonjin Shin, Myoung-Gyu Lee – Seoul National University

Measurement of Thermal, Humidity, Solder and Aging Effects of Mechanical Stress and Silicon Circuit Electrical Performance in Quad Flat Packages
Carl Philipp Riehm, Tobias Chlan, Szabolcs Molnar, Vartika Verma, Ralf Brederlow – Technical University of Munich

2025 ECTC EXHIBITION

The ECTC 2025 Exhibition is pleased to showcase dozens of companies and organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, exhibitors and attendees will enjoy continual interactions with conference attendees. We are also excited to again offer the ECTC Lounge, where attendees and exhibitors can take a few minutes to relax or converse with colleagues. Exhibit hours will be from 9:00 a.m. to 12:30 p.m. and 2:00 to 6:30 p.m. on Wednesday, May 28, 2025, and 9:00 a.m. to 12:30 p.m. and 2:00 to 4:00 p.m. on Thursday, May 29, 2025. Exhibit booths for 2025 are currently on a waitlist. Should you desire to exhibit at the 2025 ECTC, please contact samkarikalan@ieee.org or exhibits@ectc.net for getting placed on our waitlist. For additional information or questions, please contact Sam Karikalan, ECTC Exhibits Chair at +1-949-529-4802 or email samkarikalan@ieee.org and exhibits@ectc.net.

Accretech America Inc.
Adeia
Advanced Research Corp.
AI Technology
AIM Photonics
Ajinomoto Fine-Techno USA
Akrometrix
American Furukawa Inc
Amkor Technology, Inc.
AmTECH Microelectronics
AOI Electronics Co., Ltd.
AsahiKasei Corporation
ASE
ASMPT AMICRA GmbH
AT&S
Atotech / An MKS Brand
Banner Industries
Besi North America, Inc
Binghamton University / S3IP
Brewer Science
Cadence
CAMTEK USA, Inc.
Canon USA
CEA-Leti
Csun MFG, LTD
DataPhysics Instruments USA
Deca Technologies
DISCO Hi-Tec America, Inc.
DuPont Electronics & Industrial
EBINAX Co., Ltd.
ELSPES
Engent, Inc.
ERS Electronic GmbH
EV Group, Inc.
Evatec AG
F&K Delvotec Inc.
ficonTEC USA Inc.
FINECS Co., Ltd.
Finetech USA
Fraunhofer Institute for Reliability and Microintegration IZM
Fujifilm Electronic Materials, USA
GTI Technologies, Inc.
HD Microsystems
Hana Micron
Heidelberg Instruments Inc.
Henkel
Heraeus Electronics
IBM
Indium Corporation
Institute of Microelectronics, A*STAR Singapore
Intekplus
Intel Corporation
JIACO Instruments
JSR Micro, Inc.
JX Advanced Metals
KLA Corporation
Kleindiek Inc.
Koh Young Technology, Inc.
Kulicke and Soffa Industries Inc.
Kyocera International, Inc.
Lam Research
Laser Thermal Analysis
Lintec of America, inc.
LPKF Laser & Electronics
LQDX Inc.
MEC Company Ltd.
Micro.electronics
Microcircuit Laboratories LLC
Micross Components
Mini-Systems Inc.
Mitsubishi Materials USA Corporation
Mitsui Chemicals America
MKElectron Co., Ltd.
Nagase ChemteX Corporation
NAMICS Technologies, Inc.
Neu Dynamics Corp.
Niching Industrial Corporation
Nova Ltd.
nScrypt
OKUNO Chemical Industries Co., Ltd.
Onto Innovation
PacTech USA
Panasonic Industrial Devices Sales Company of America
Parmi USA
PLANOPTIK AG
Plasmatreat North America, Inc.
QML, Inc.
QP Technologies
QualiTau
RENA Technologies GmbH
Resonac
Royce Instruments (V-TEK, Inc.)
S-Cubed
Samtec
Sanyu Rec Co., Ltd.
SavanSys Solutions LLC
SawStreet
Scientech Corp.
SCREEN Holdings Co., Ltd.
SEKISUI Chemical Co., Ltd.
Semiconductor Equipment Corp.
Senju Comtek Corp (SMIC)
SETNA
Shikoku Chemicals Corporation
Shin-Etsu MicroSi
Shinkawa USA Inc.
Shinko Electric America, Inc.
Sigray
SkyWater Technology
Smart High Tech
Sono-Tek
Stats ChipPAC
STRAMATEC
Surfx Technologies
SUSS MicroTec Inc.
Taiyo Ink Mfg. Co., Ltd.
Tazmo Inc.
TDK Corporation of America
Technic
TechSearch International, Inc.
TEL
Tokyo Electron, Ltd.
Tokyo Ohka Kogyo Co., Ltd.
Toray International America Inc.
TOWA USA Corporation
Toyochem Co., Ltd.
Toyota Tsusho America, Inc.
Ushio Inc.
XTPL, Inc.
XYZTEC, Inc.
ZEISS Microscopy
Zuken USA Inc.
Zymet, Inc.

AREA ATTRACTIONS

Located in Grapevine Texas, the Gaylord Texan Resort & Convention Center welcomes guests to a stunning, one-of-a-kind experience. From the seasonal 10-acre Paradise Springs Water Park to an exciting lineup of family-friendly activities and entertainment, there's something for the entire family to enjoy at the Gaylord Texan. Guests can explore the four-and-a-half acres of airy, indoor garden atriums, four award-winning restaurants, bars, the world-class Relâche Spa and a state-of-the-art fitness center. The hotel also offers 1,814 beautiful guest rooms, and 127 spectacular suites, along with our lakeside event venue, the Glass Cactus, perfect for live entertainment & events. With prime location near DFW Airport, LEGOLAND® Discovery Center, Cowboys Golf Club, and Historic Downtown Grapevine, do more of what you love at Gaylord Texan Resort & Convention Center.

HOTEL RESERVATIONS

Gaylord Texan Resort & Convention Center
1501 Gaylord Trail • Grapevine, TX 76051

Hotel reservations for ECTC 2025 can be made one of two ways:

1) Contact the Gaylord Texan Resort & Convention Center at +1 (817) 778-1000 and reference the ECTC Conference to receive the conference rate of US $229 per night.

or …

2) Log onto **www.ectc.net** and click on the Location tab near the top of the page to find a special online hotel registration link.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2025 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2025 from third-party companies. These emails and sites are not to be trusted. **The only formal communication ECTC** will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC's only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: **registration@ectc.net**

HOW TO REGISTER FOR ECTC:

By Internet: Submit your registration electronically via www.ectc.net. Your registration must be received by the cutoff date, May 1, 2025, to qualify for the early registration discounts.

You may contact our registration staff at **registration@ectc.net** for additional information. Payment can be made by Visa, Mastercard, Discover, or American Express.

75th Electronic Components & Technology Conference

2025 ECTC REGISTRATION INFORMATION

Conference Registration		Advance Registration Until May 1	Door Registration Starting May 2
IEEE Member	Attendee (full ECTC conference)	US $1100	US $1265
	Attendee (Joint ECTC + ITHERM conferences)	$1430	$1665
	Attendee One-Day Registration	$835	$835
	Speaker or Chair (full ECTC conference)	$935	$1135
	Speaker or Chair One-Day Registration	$735	$735
Non-IEEE Member	Attendee (full ECTC conference)	$1365	$1530
	Attendee (Joint ECTC + ITHERM conferences)	$1665	$1995
	Attendee One-Day Registration	$835	$835
	Speaker or Chair (full ECTC conference)	$935	$1135
	Speaker or Chair One-Day Registration	$735	$735
Student	Attendee or Speaker (full conference)	$455	$455
Professional Development Courses (PDCs)			
IEEE Member	Full PDC (both a.m. and p.m.)	$625	$625
	Single PDC (a.m. or p.m.)	$440	$440
Non-IEEE Member	Full PDC (both a.m. and p.m.)	$675	$675
	Single PDC (a.m. or p.m.)	$490	$490
Student	Full PDC (both a.m. and p.m.) or Single PDC	$150	$150
Other Registration Options			
Extra Luncheon Tickets		$100	$100
Cancellation Fee		$100	$100

Please note that we are no longer offering the purchase of an extra copy of the proceedings. Additionally, the various exhibit registration types are no longer available for the general public.

Please log onto www.ectc.net/registration to register for 2025 ECTC.

There will be no refunds or cancellations after May 1, 2025. Please note that a $100 cancellation fee will be in effect for all cancellations made on or prior to May 1, 2025. Substitutions can be made at any time.

For additional information about registration or ECTC please contact us at:

ECTC Registration
% Renzi & Company, Inc. Management
Email: registration@ectc.net

If you join IEEE **BEFORE you register for the 2025 ECTC you can save on registration fees and get the Electronics Packaging Society (EPS) add-on membership free for the reminder of the year!*

To take advantage of this offer, simply go to: https://www.ieee.org/membership-application/public/join.html

At destination, create your IEEE Web Account and proceed with the IEEE Membership Application. Enter the promotion code EPS2025ECTC in the promotion code box before payment. Use your new IEEE membership ID number and register for ECTC at the discounted IEEE Member Rate.

If you are already an IEEE member, you can add EPS membership for free using the same promotion code.

CONFERENCE SPONSORS

PLATINUM

amkor.com

aseglobal.com

ibm.com/consulting/assembly-test-service

GOLD

adeia.com

asahi-kasei.com

atotech.com/usa

brewerscience.com

ThinkDeca.com

dupont.com/electronic-materials

evgroup.com

evatecnet.com

hanamicron.com

henkel-adhesives.com/us/en/industries/electronics.html

intekplus.com

intel.com/content/www/us/en/foundry/packaging.html

kla.com

lamresearch.com

marvell.com

micross.com

group.nagase.com

nagasechemtex/en/namics-corp.com

pactech.com

semiconductor.samsung.com

spil.com.tw

suss.com

tel.com

tsmc.com

yieldengineering.com

SILVER

ajinomoto.com

screen.co.jp

statschippac.com

tokamerica.com

mds.umicore.com/en/

uyemura.co.jp

CONFERENCE SPONSORS

GALA RECEPTION SPONSOR

kohyoung.com

REGISTRATION SPONSOR

zymet.com

BADGE LANYARD

hdmicrosystems.com

STUDENT RECEPTION

ti.com

PEN SPONSOR

qml.us

STUDENT BEST PAPER SPONSOR

intel.com

PROGRAM SPONSOR

utechzone.com.tw/index_en.php

PANEL SESSIONS SPONSOR

binghamton.edu/s3ip

rapidus.inc

fujifilmusa.com

usiglobal.com

zymet.com

CONFERENCE APP SPONSOR

zymet.com

COFFEE CUP SPONSOR

kla.com

REFRESHMENT BREAK SPONSORS

fujifilmusa.com

rena.com

utdallas.edu

mds.umicore.com/en/

MEDIA

Official Media Sponsor

chipscalereview.com

Additional Media Sponsors

3dincites.com

circuitsassembly.com

eptc-ieee.net

laserfocusworld.com

meptec.org

pcbdirectory.com

pcea.net

semiconductor-digest.com

semiengineering.com

semiconductorpackagingnews.com

yole.fr

CONFERENCE OVERVIEW

TUESDAY, MAY 27, 2025

Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.

1. Design of Reliable Data Center Cooling Systems
2. Eliminating Failure Mechanisms in Advanced Packages
3. From Wafer to Panel Level Packaging
4. High Reliability Soldering in Semiconductor Packaging
5. Introduction to and Advances in 2.3D Fan-Out Wafer Level Packaging (FO-WLP)
6. Photonic Technologies for Communication, Sensing, and Displays
7. Polymers for Advanced Packaging
8. Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Advanced Interconnects

ECTC Special Sessions
8:30 a.m. - 10:00 a.m.

1. Hybrid Bonding (HB): to B, or not to B? Needs and Challenges for the Next Decade
2. Ultra High-Density Interconnect Technologies and Supply Chain Readiness for AI & HPC
3. IoT and AI at the Edge (HIR)

ECTC Special Sessions
10:30 a.m. - 12:00 p.m.

1. Glass Core vs. RDL Interposers: Ready for Prime Time?
2. Quantum Photonics Advanced Packaging
3. Advancing Heterogeneous Integration through Metrology and AI (HIR)

Afternoon Professional Development Courses
1:30 p.m. - 5:30 p.m.

9. 3D Packaging Failure Analysis - Failure Mechanisms and Analytical Tools
10. Advanced Fan-Out Developments and Applications
11. Analysis of Fracture and Delamination in Microelectronic Packages
12. Chiplet, Heterogeneous Integration, and Co-Packaged Optics
13. Current and Future Challenges and Solutions in AI & HPC System and Thermal Management
14. Design-On-Simulation for Advanced Packaging Reliability and Life Prediction
15. Diamond for Heterogeneous Integration
16. Flip Chip Technologies

Tuesday Luncheon
12:00 Noon – 1:15 p.m.

ECTC Special Sessions
1:30 p.m. - 3:00 p.m.

1. Advanced Materials for Enabling Co-Packaged Optics Integration
2. Advances in Chiplets; Tackling Fault Isolation and Failure Analysis in Heterogeneous Integration
3. Integrating Photonics in HPC and Network Systems (HIR)

ECTC Special Sessions
3:30 p.m. - 5:00 p.m.

1. Advancements in mm-Wave and Sub-THz Packaging for Communication and Radar Applications
2. Thermal Management Solutions for Next-Generation Backside Power Delivery
3. Innovations in Panels, Substrate and Printed Circuit Boards (HIR)

Young Professionals Networking Panel
7:00 p.m. - 7:45 p.m.

ECTC EPS Seminar
7:45 p.m. - 9:15 p.m.
User Perspective of Chiplet Technology

WEDNESDAY, MAY 28, 2025

ECTC Keynote
8:00 a.m. - 9:15 a.m.
Achieving Efficient Zettascale Compute in the AI Era

Technical Sessions
9:30 a.m. - 12:35 p.m.

1. Processing and Packaging Articles for 3D Integration
2. Co-Packaged Optics
3. Hybrid Bonding Materials and Processing for Advanced Packaging
4. Large Package Manufacturing and Panel Level Processing
5. Advanced Design for Heterogeneous Integration
6. AI - ML and Emerging Modeling Methods

Interactive Presentation Session 37
10:00 a.m. - 12:00 p.m.

Wednesday Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

7. High Performance Computing and Design Challenges and Solutions
8. Novel Structures and Processes for Chip-to-Wafer Hybrid Bonding
9. Co-Packaged Optics and Hybrid Bonding Innovations for Heterogeneous Integration
10. High Reliability Applications
11. Emerging Trends: Towards High Speed, Secure, Reliable, and Sustainable Packaging
12. Advanced Thermal Management Modeling

Interactive Presentation Session 38
2:30 p.m. - 4:20 p.m.

ECTC Student & Start-up Innovation Challenge
6:30 p.m. - 8:30 p.m.

THURSDAY, MAY 29, 2025

ECTC Plenary Session
8:00 a.m. - 9:15 a.m.
Emerging Advanced Power Delivery for the AI Computing Era

Technical Sessions
9:30 a.m. - 12:35 p.m.

13. Large Panel Fan-Out for High Density Integration
14. New Materials and Processes in Wafer-to-Wafer Hybrid Bonding
15. Photonics Integration and Subsystems
16. Manufacturing and Thermal Management Reliability
17. Signal Integrity / Power Integrity for Advanced Packaging Technologies
18. Simulations and Validation on Reliability Challenges of High Performance Packages

Interactive Presentation Session 39
10:00 a.m. - 12:00 p.m.

Thursday EPS Awards Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

19. Chiplet Integration and Advanced Thermal Solutions
20. Novel Technologies for High Density RDL Interposers
21. Meeting AI Challenges : Large Package Solution and Warpage Management for Advanced Packaging
22. Heterogeneous Integration Using Bridge and 3D Stacking
23. AI Enabled Innovations in Advanced Packaging Technologies
24. Advanced Characterization and Modeling of Next Generation Packaging Materials

Interactive Presentation Session 40
2:30 p.m. - 4:20 p.m.

FRIDAY, MAY 30, 2025

ECTC EPS President's Panel: ECTC at 75: Celebrating the Past, Innovating for the Future
8:00 a.m. - 9:15 a.m.

Technical Sessions
9:30 a.m. - 12:35 p.m.

25. Advanced Substrate Technologies - Organic, Embedding and Glass
26. Process Innovation in Through-Via and Solder Interconnections
27. Thermal Management and Material Solutions for High Performance 2.5D and 3D Packaging
28. Reliability of Heterogeneous Integrated Packages
29. Advances in Additive Manufacturing, Wearable and Medical Technologies
30. Simulations on Advanced Package Processing - Hybrid Bonding, Chip Stacking and Wafer-to-Wafer

Student Interactive Presentations Session 41
10:00 a.m. - 12:00 p.m.

Raffle Prize Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

31. Automotive Power
32. Design, Materials, Metrology & Standards for Next Generation Interconnections
33. Innovative Interconnects and Through Via Technology for 3D Packaging
34. Reliability of Interconnects in Advanced Packaging
35. High-Performance Antenna and RF Design
36. Modeling Driven Packaging and Process Advancements

Session Summary by Interest Area

Packaging Technologies
S1, S7, S13, S19, S25, S31

Applied Reliability
S10, S16, S28, S34

Assembly & Manufacturing Technology
S4, S22

Emerging Technologies
S11, S29

Electrical Design and Analysis
S5, S17, S23, S35

Interconnections
S8, S14, S20, S26, S32

Materials & Processing
S3, S9, S21, S27, S33

Thermal/Mechanical Simulation & Characterization
S6, S12, S18, S24, S30, S36

Photonics
S3, S15

Interactive Presentations
S37, S38, S39, S40, S41

The 2025 IEEE 75th Electronic Components and Technology Conference

IEEE EPS
445 Hoes Lane, Piscataway, NJ 08854-4141 USA

Mailroom: If the person on this label is no longer employed at your company, please route this information brochure to his/her replacement or department manager.

Route to: _____

_____

Attn: Engineers, scientists and technical managers

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

Program Supported by

UH UTECHZONE

FIRST CLASS
U.S. POSTAGE
PAID
RALEIGH, NC
PERMIT NO. 2172

Advance Registration through May 1, 2025
For more information, visit: www.ectc.net

Mark your calendar for ECTC 2025!

Gaylord Texan Resort & Convention Center

Dallas, Texas, USA

May 27 – May 30, 2025