Modeling of CTE Mismatch Effects in Multi-Material Packages

Context:

With the growing adoption of heterogeneous integration and advanced materials in semiconductor packaging, managing thermal expansion mismatches remains a cornerstone challenge for ensuring package integrity and long-term reliability. Teams must develop advanced simulation models to predict and mitigate the effects of CTE mismatch in packages utilizing multiple materials

Challenge:

- Conduct detailed study of CTE mismatch effects in packages with multiple materials and identify key challenges that arise due to the mismatch in thermal expansion coefficients between materials.
- Select materials and define the package structure, including interfaces where CTE mismatch would most likely cause stresses.
- Develop a 3D model of the package using FEA tools and simulate thermal expansion under extreme boundary conditions (-40°C/ +85°C)
- Based on the simulation results, identify regions in the package most prone to failure.

If you select this challenge, use in the emails title code: **Ch2**

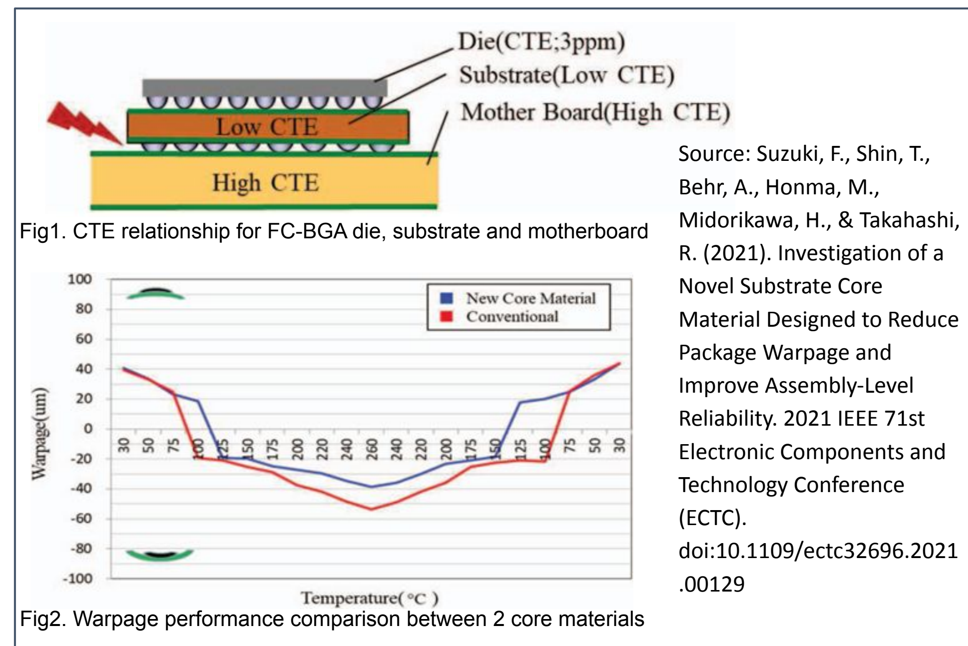

Fig1. CTE relationship for FC-BGA die, substrate and motherboard

Fig2. Warpage performance comparison between 2 core materials

Source: Suzuki, F., Shin, T., Behr, A., Honma, M., Midorikawa, H., & Takahashi, R. (2021). Investigation of a Novel Substrate Core Material Designed to Reduce Package Warpage and Improve Assembly-Level Reliability. 2021 IEEE 71st Electronic Components and Technology Conference (ECTC). doi:10.1109/ectc32696.2021.00129

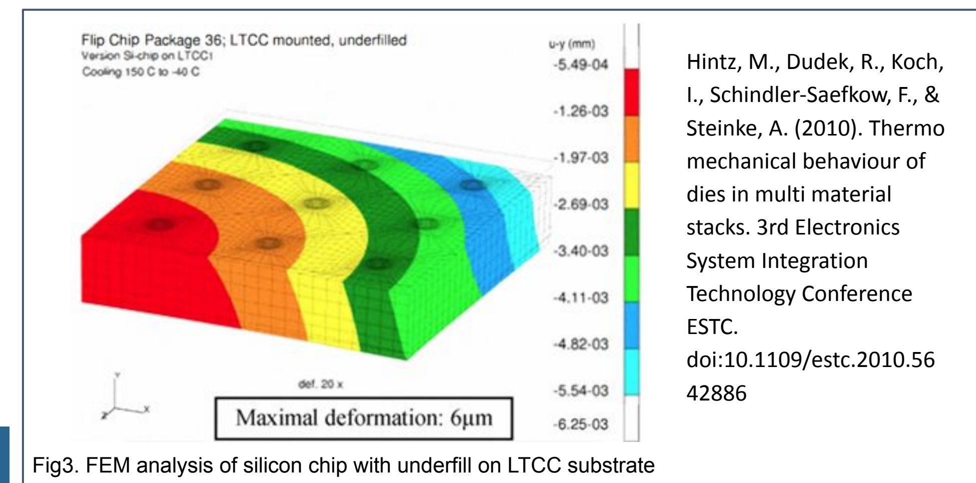

Fig3. FEM analysis of silicon chip with underfill on LTCC substrate

Hintz, M., Dudek, R., Koch, I., Schindler-Saefkow, F., & Steinke, A. (2010). Thermo mechanical behaviour of dies in multi material stacks. 3rd Electronics System Integration Technology Conference ESTC. doi:10.1109/estc.2010.5642886